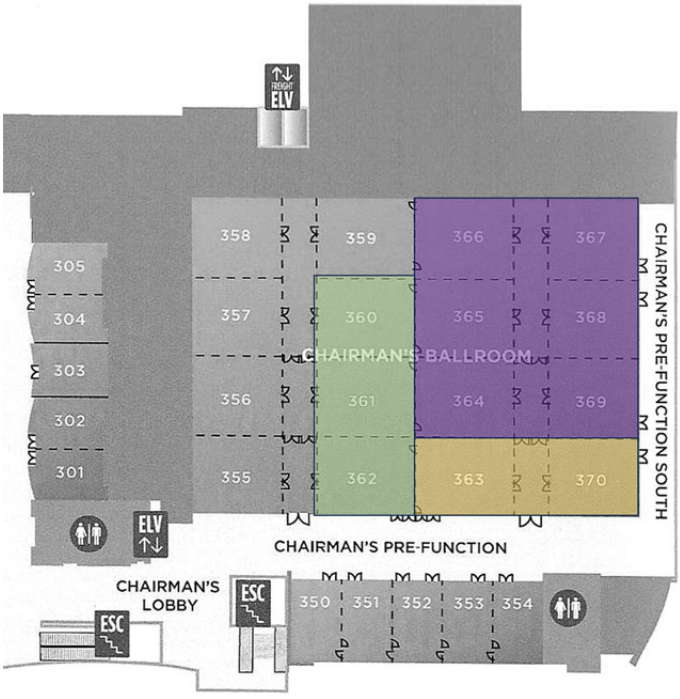
MGM GRAND CONFERENCE CENTER

3RD FLOOR DIRECTORY



Poster Area

Exhibitor & Coffee Break Area

Main Lecture Hall

SCHEDULE AT A GLANCE

Time	Sun - May 24	Mon - May 25
8:30		**Opening Session** 8:30 - 9:00
9:00	**Short Course 1** 9:00 - 10:00	**Plenary Session (2)** 9:00 - 10:20
9:30		
10:00	**Short Course 2** 10:00 - 11:00	**Coffee** 10:20 - 10:40
10:30		**HV-1 (4)** 10:40 - 12:00
11:00	**Short Course 3** 11:00 - 12:00	
11:30		
12:00	**Lunch** 12:00 - 13:30	**Lunch** 12:00 - 13:30
12:30		
13:00		
13:30	**Short Course 4** 13:30 - 14:30	**SiC-1 (5)** 13:30 - 15:10
14:00		
14:30	**Short Course 5** 14:30 - 15:30	
15:00		**Coffee** 15:10 - 15:30
15:30	**Short Course 6** 15:30 - 16:30	**GaN-1 (5)** 15:30 - 17:10
16:00		
16:30		
17:00		
17:30		
18:00		**Welcome Reception** 18:00 - 20:00
18:30		
19:00		
19:30		

SCHEDULE AT A GLANCE

Time	Tue - May 26	Wed - May 27
8:30		
9:00	**LVT-1 (4)** 8:40 - 10:00	**HV-2 (4)** 8:40 - 10:00
9:30		
10:00	**Coffee** 10:00 - 10:20	**Coffee** 10:00 - 10:20
10:30	**SiC-2 (5)** 10:20 - 12:00	**Ga203 (5)** 10:20 - 12:00
11:00		
11:30		
12:00	**Lunch** 12:00 - 13:30	**Lunch** 12:00 - 13:30
12:30		
13:00		
13:30	**ICD (4)** 13:30 - 14:50	**PK (5)** 13:30 - 15:10
14:00		
14:30		
15:00	**GaN-2 (4)** 14:50 - 16:10	**Coffee** 15:10 - 15:30
15:30		**Poster 2** 15:30 - 17:00
16:00	**Coffee** 16:10 - 16:30	
16:30	**Poster 1** 16:30 - 18:00	
17:00		
17:30		
18:00		
18:30		
19:00		**Banquet Hall of Fame** 19:00 - 22:00
19:30		

SCHEDULE AT A GLANCE

Time	Thu - May 28
8:30	**SiC-3 (4)** 8:40 - 10:00
9:00	
9:30	
10:00	**Coffee** 10:00 - 10:20
10:30	**GaN-3 (5)** 10:20 - 12:00
11:00	
11:30	
12:00	**Lunch** 12:00 - 13:30
12:30	
13:00	
13:30	**LVT-2 (4)** 13:30 - 14:50
14:00	
14:30	
15:00	**Closing Session** 14:50 - 15:20
15:30	
16:00	
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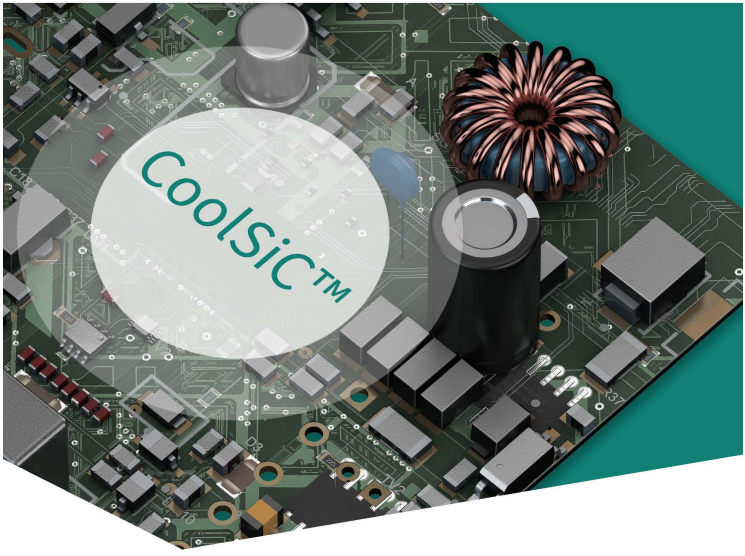

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GENERAL CHAIR'S MESSAGE

Dear Colleagues,

On behalf of the Organizing Committee, it is my privilege to welcome you to the 38th International Symposium on Power Semiconductor Devices and ICs (ISPSD 2026). After a four year international rotation, ISPSD will return to North America in the energetic city of Las Vegas, Nevada on May 24 – 28, 2026. This premier global forum brings together leading researchers, academics, and industry professionals to share groundbreaking advancements, exchange innovative ideas, and shape the future of power semiconductor devices and integrated circuits.

I am very pleased that we can offer the conference as an in-person format to allow the face-to-face engagements that are at the heart of ISPSD 2026. Our program features a specialized short course, distinguished keynote addresses, rigorous technical sessions, and a wonderful social program. These interactions during the technical sessions, questioning results in front of a poster, or lively debates during a social hour—are intended to spark further developments in our field.

The conference location, Las Vegas, is routinely ranked as one of the top locations for conferences in the world. Its central location with a major international airport, will make it easily accessible for all of our global attendees. Beyond logistics, the city has a various range of dining and entertainment, and direct access to amazing natural wonders like the famous Grand Canyon National Park.

As the paper submission format has now changed to a 4-page full paper, please plan your research accordingly to take advantage of this great conference. I look forward to welcoming you to Las Vegas for ISPSD 2026!

Sincerely,

Dr. David Sheridan
General Chairman, ISPSD 2026

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GENERAL INFORMATION

Conference Venue
MGM Grand Conference Center
4701 Koval Ln, Las Vegas, NV 89109
https://www.mgmgrand.com/

Recording and Photography Policy
IEEE policy **prohibits** video recording or photographing of presentations unless permission from the presenter is obtained in advance. Photographing of people or social events is permitted.

SOCIAL EVENTS

Monday Welcome Reception
Date & Time: Monday, May 25, 18:00–20:00
Venue: MGM Conference Center – 3rd Floor - Chairman's Ballroom
Included in registration fee

Banquet
Date & Time: Wednesday, May 27, 19:00–22:00
Venue: MGM Conference Center – 3rd Floor – Premier Pre-Function
Entertainment: Magician Lou Serrano
Included in registration fee

About Lou Serrano: Lou Serrano is a corporate magician and mentalist who performs for conferences, leadership meetings, and corporate events around the world. His performances combine sophisticated magic, interactive mind reading, and comedy to create unforgettable shared experiences for audiences of all sizes. Known for engaging even the most analytical minds, Lou's performances spark curiosity, laughter, and genuine astonishment, leaving audiences talking long after the event ends.

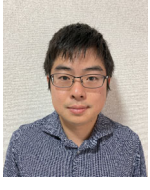
ISPSD2025
Ohmi Best Paper Award

GaN/SiC-Based Polarization Superjunction Hybrid HEMTs (PSJ-hyHEMTs) on Vicinal Off-Angle SiC

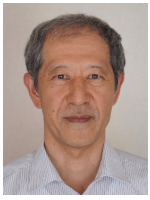
Akira Nakajima*, Hirohisa Hirai, Yoshinao Miura,
Kazutoshi Kojima, Tomohisa Kato, and Shinsuke Harada
Advanced Power Electronics Research Center (ADPERC), National Institute of Advanced Industrial Science and Technology (AIST),
Tsukuba, Ibaraki, Japan

Abstract:
GaN/SiC-based Polarization Superjunction hybrid HEMTs (PSJ-hyHEMTs) have been demonstrated. The PSJ-hyHEMTs were fabricated on 4-inch SiC substrates with a vicinal off-angle (0.65° off) to reconcile the crystal growth of both GaN and SiC. The avalanche breakdown voltage of the SiC-based body PiN diodes was designed at 1.2 kV by TCAD. GaN-based PSJ-HEMTs were monolithically integrated on top of the SiC diodes. The fabricated GaN/SiC-based PSJ-hyHEMTs show normally-off operation with threshold voltage of 0.5 V, low-specific on-resistance of 24 Ω·mm, and non-destructive avalanche breakdown at 1.2 kV. These fusion technologies of GaN and SiC could be promising candidates as next-generation devices beyond current GaN and SiC devices.

Akira Nakajima received his B.E., M.E., and Ph.D. degrees from Toyohashi Institute of Technology in 2000, 2002, and 2005, respectively. He joined the National Institute of Advanced Industrial Science and Technology (AIST) in 2005, where he has been engaged in research on power semiconductor devices. From 2009 to 2011, he was a Newton International Fellow at the University of Sheffield. Since 2011, he has been serving as a Senior Researcher at AIST. He is currently focused on the development of GaN-based power ICs and the integration of GaN and SiC power device technologies.



Hirohisa Hirai received his B.E., M.E., and Ph.D. degrees in the Department of Materials Engineering, from the University of Tokyo, Japan, in 2013, 2015, and 2018, respectively. Since 2018, he has been with the Advanced Power Electronics Research Center at AIST. His research interests include MOS interface engineering, MOSFET development, and heterogeneous integration of widegap semiconductor devices.



Yoshinao Miura received the B.E. and M.E. degrees in the University of Tokyo, in 1988 and 1990, respectively. In 1990, he joined NEC Corporation and engaged in the fields of material characterization for Si devices and development of power devices. In 2006, he received the Ph.D. degree from the University of Tokyo. Since 2018, he has been working in the National Institute of Advanced Industrial Science and Technology (AIST). His research interest includes nitride power devices.

Kazutoshi Kojima received his Ph.D. in materials science from the University of Tsukuba in 1997. He began research and development on 3C-SiC epitaxial growth technology at JAEA (currently QST) in the same year. In 2000, he shifted his R&D focus from 3C-SiC to 4H-SiC at the National Institute of Advanced Industrial Science and Technology (AIST), where he has continued to work on 4H-SiC epitaxial growth technology for over 25 years.

Tomohisa Kato obtained his PhD in Materials Engineering from Nagoya Institute of Technology in 1999. From April 1999, he worked at the National Institute of Advanced Industrial Science and Technology (AIST), developing SiC single crystal growth and wafer processing technologies. He served as Wafer Theme Leader for two NEDO projects in 2010 and 2014, and has overseen SiC wafer development within the TPEC consortium since 2019.

Shinsuke Harada received the B.S., M.S., and Ph.D. degrees in materials science and engineering from Kyushu university, Fukuoka, Japan, in 1995, 1997, and 2000. He is currently a deputy director of Advanced Power Electronics Research Center of National Institute of Advanced Industrial Science and Technology (AIST) in Japan. His current research interests include SiC power devices development such as MOSFET, superjunction, IGBT, power IC, and hybrid devices with GaN.

ISPSD2025
Charitat Young Researcher Award

First Demonstration of a Fully-Vertical GaN Power finFET with Direct Optical Triggering

Jung-Han Hsia[1]*, Joshua Andrew Perozek[1],
Joseph Park[2], and Tomas Palacios[1]*

[1]Microsystems Technology Laboratories,
Massachusetts Institute of Technology, Cambridge, MA, USA
[2]MIT Lincoln Laboratory, Lexington, MA, USA

Abstract:
Optically controlled power devices hold immense promise for enabling next-generation high-voltage systems with enhanced performance and simplified architectures. In this work, we present a fully vertical, optically triggered GaN finFET directly driven by a UV LED. The device achieves a remarkable optical gain of $R > 10^4$ A/W, a robust current on-off ratio of $I_{on}/I_{off} > 10^7$, and a low specific on-resistance of $R_{on,sp} = 60$ $m\Omega cm^2$ under an optical power density as low as $P_{LED} = 17$ mW/cm^2. Furthermore, it demonstrates an off-state breakdown voltage BV > 600V. A single, large area device with $R_{on} = 2.6\Omega$ was also successfully demonstrated. These results highlight the significant potential of this device to mitigate electromagnetic interference (EMI) and simplify gate driver design in high-voltage electronics, paving the way for cost effective, high-efficiency optically controlled power systems with innovative topologies.

Jung-Han Hsia received the B.S. in Materials Science and Engineering from the University of California, Berkeley, in 2021, and the M.S. in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology (MIT) in 2023. She is currently a Ph.D. candidate in Electrical Engineering and Computer Science at MIT. Her research interests include GaN power semiconductor devices, device modeling, and advanced semiconductor fabrication and integration technologies.

ISPSD2025
Best Poster Award

Low ON-Resistance Vertical GaN-on-GaN Trench MIS-FET with Small Temperature Dependence

Zaitian Han, Hao Zhang, Shibing Long and Shu Yang*

School of Microelectronics,
University of Science and Technology of China,
Hefei, China

Abstract:
In this work, we demonstrate a high-performance normally-off vertical GaN-on-GaN trench MIS-FET featuring a low ON-resistance and small temperature dependence. The gate trench optimization can effectively suppress surface roughness scattering along the trench sidewall, whereby the inversion channel mobility can be boosted from 70 $cm^2/V{\cdot}s$ (without gate trench optimization) to 210 $cm^2/V{\cdot}s$. Thanks to the enhanced channel mobility, the 1.4 kV vertical GaN trench MIS-FET can deliver a low specific ON-resistance ($R_{ON,sp}$) of 2.0 $m\Omega{\cdot}cm^2$ with a low channel resistance percentage ($R_{ch}/R_{ON,sp}$) of ~10%, along with a desirably high threshold voltage (V_{TH}) of 3.9 V at room temperature. Furthermore, within a wider temperature range (−75–125 ^oC), the vertical GaN MIS-FET can maintain a normally-off operation with a small temperature dependence of V_{TH} and $R_{ON,sp}$, showing great potential for high-efficiency and high-temperature power electronics applications.

Zaitian Han received the B.E. degree in microelectronics science and engineering from Anhui University, Hefei, China, in 2022. He is currently pursuing the Ph.D. degree with the School of Microelectronics, University of Science and Technology of China, Hefei, China. His current research interests include fabrication and characterization of GaN-based power transistors.

Hao Zhang received the B.E. degree from Hefei University of Technology, Hefei, China, in 2024. He is currently pursuing the M.S. degree with the School of Microelectronics, University of Science and Technology of China, Hefei, China. His research focuses on the design and fabrication of GaN power devices.

Shibing Long is a full professor at the School of Microelectronics, University of Science and Technology of China. He received his Ph.D. degree from the Institute of Microelectronics of the Chinese Academy of Sciences in 2005. Then, he worked there from 2005 to 2018 and joined the University of Science and Technology of China in 2018. His research focuses on micro and nanofabrication, RRAM, ultrawide bandgap semiconductor devices (power devices and detectors) and memory circuit design.

Shu Yang is a full professor at the School of Microelectronics, University of Science and Technology of China. She received her B. S. degree from Fudan University, and her Ph.D. degree from the Hong Kong University of Science and Technology (HKUST) with PhD Research Excellence Award. She was a visiting assistant professor at HKUST, a post-doctoral research associate at the University of Cambridge and a professor at Zhejiang University. Her research interests include fabrication, characterization and application-relevant study of GaN-based power devices. Dr. Yang was a recipient of IEEE ISPSD Charitat Young Researcher Award.

Michael S. Adler for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Gehan Anil Joseph Amaratunga for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

B. Jayant Baliga for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Xingbi Chen* for his contributions to superjunction power semiconductor devices

Tat-Sing Paul Chow for his contributions to silicon and wide bandgap power semiconductor devices, and his leadership role in organizing ISPSD conferences

Claudio Contiero for his contributions to the proliferation of BCD technologies, and to the ISPSD conferences

Mohamed Darwish for his contributions to the advancement of power semiconductor technology, and his leadership role in organizing ISPSD conferences

Don Disney for contributions to power IC technology, and his leadership role in organizing ISPSD conferences

Taylor R. Efland for his contributions to power IC technology, and his leadership role in organizing ISPSD conferences

Wolfgang Fichtner for his contributions to MOS gated thyristors and TCAD modeling tools, and his leadership role in organizing ISPSD conferences

Peter Friedrichs† for his significant and outstanding contribution to the proliferation of SiC power semiconductor devices

Tatsuhiko Fujihira for his contributions to superjunction power semiconductor technologies and industrialization of power semiconductor devices

Oliver Häberlen for his contributions to trench MOSFET and power GaN technology, and for his outstanding leadership in organizing ISPSD 2020 during the pandemic

Kimimori Hamada† for his contributions to the development of power semiconductor devices for hybrid electric vehicles and for leadership of ISPSD 2021 conference during the pandemic

Min-Koo Han for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Phil Hower for his contributions to power device safe operating area study and power IC technology

André A. Jaecklin for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Daniel Kinzer for his contributions to power MOSFET technology, and his leadership role in organizing ISPSD conferences

Thomas Laska for his contributions to IGBT technology and devices

Alex Lidow for contributions to silicon and GaN power device technology

Leo Lorenz for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Gourab Majumdar for his contributions to IGBT and intelligent power module technology, and his leadership role in organizing ISPSD conferences

Hiroyuki Matsunami for his contributions to the developments of silicon carbide epitaxial technology and wide bandgap power semiconductor devices

José Millán* for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Peter Moens for his contributions to integrated power technology and GaN power device and reliability, and his leadership role in organizing ISPSD conferences

Mutsuhiro Mori for his contributions to high voltage insulated gate bipolar transistor for traction and high voltage systems, and his leadership role in organizing ISPSD conferences

Akio Nakagawa for his contributions to IGBT and power IC technology

Hiromichi Ohashi for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Tadahiro Ohmi* for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Masahiro Okamura for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

John Palmour* for his contributions to SiC technology and devices

James Plummer for his contributions to MOS-bipolar power devices and power ICs, and for inspiring and training a new generation of device researchers

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John Shen for contributions to high-frequency power MOSFET and leadership role in organizing ISPSD

Kuang Sheng for his contributions to SiC power device technology, and his leadership role in organizing ISPSD conferences

M. Ayman Shibib for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Dieter Silber for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Johnny Sin for his contributions to the design and commercialization of power semiconductor devices and his leadership role in organizing ISPSD conferences

Jan Šonský for his contributions to GaN device technology, and his leadership role in organizing ISPSD conferences

Paolo Spirito for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Yoshitaka Sugawara for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Yoshiyuki Uchida for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

Florin Udrea for inspiring a generation of engineers to excel in power semiconductors and his numerous contributions to the field and to ISPSD

Daisuke Ueda for his work on trench structure MOS devices and GaN devices

Harry Vaes for his contributions to RESURF technology

Jan Vobecký for pushing the limits of diodes and thyristors by carrier lifetime engineering

Carl Frank Wheatley* for his contributions to IGBT and radiation-hard power device technology

Richard K. Williams for his contributions to trench power MOSFET and power IC technology, and his leadership role in organizing ISPSD conferences

Toshiaki Yachi for his contributions to modern power semiconductor technology, and his leadership role in organizing ISPSD conferences

* Deceased member

† New inductees for 2026

Power Delivery as the Limiting Factor in AI Systems: From Transistor Scaling to Rack-Scale Power Architecture

Dr. Ahmed Abou-Alfotouh, *AMD, USA*

Abstract: As AI systems scale from advanced semiconductor nodes to rack-level deployments approaching megawatt power, power delivery has become a primary limiter of performance, efficiency, and reliability. Extreme current densities, shrinking voltage margins, and fast load transients expose fundamental limits of traditional low-voltage and lateral power architectures, creating a growing misalignment between logic scaling and power device evolution. This work examines the system-level breakdown of conventional power delivery approaches and highlights the need for vertical power delivery, higher-voltage distribution, and system-aware power semiconductor design across device, package, board, and infrastructure levels. A renewed research mandate is proposed for the ISPSD community, emphasizing physics-grounded, system-level co-design to enable continued AI performance scaling.

Biography: Dr. Abou-Alfotouh is the chief Power Architect at AMD (Advanced Micro Devices), focusing on datacenter GPU and accelerated processing technologies. He previously held a similar role at NVIDIA and Intel. Ahmed finished his Ph.D. in Power Electronics from University of Kentucky with 26+ Industry experience. He holds patents and has published research on topics such as power converters and semiconductor characterization. He is currently focusing on improving data center power delivery efficiency and density.

Power Electronics Systems for Heavy-Duty Off-Road Vehicles

Dr. Brij Singh, *John Deere, USA*

Abstract: This presentation discusses publicly available information related to vehicle electrification projects at John Deere, highlighting several enabling technologies developed within the company. The scope includes high-power converters based on both silicon (Si) IGBTs and silicon carbide (SiC) MOSFETs, including a 200 kW, 1050 VDC silicon carbide (SiC) dual inverter. The front-end converter architecture, which transforms mechanical power from the vehicle engine into electrical power for the electric powertrain, will be described with a focus on heavy-duty construction and agricultural vehicles. The presentation covers the development and test verification of key technologies that enabled the successful realization of a power-dense (43 kW/L), high-temperature inverter suitable for operation with 115 °C water-ethylene-glycol coolant, while achieving high efficiency (>98% across the entire coolant temperature range). In addition, a brief overview of 700V 100kW soft-switching SiC (S2SiC) inverter technology will be provided.

Biography: Dr. Brij Singh (Fellow IEEE) is John Deere Technical Fellow in Power Electronics Engineering and serving as the Electrification R&D Manager in John Deere USA. He has authored or coauthored 105 research papers, 41 granted US patents, and one trade secret. His current research interests include wide bandgap technologies, power electronics for precision agriculture, vehicles' electrification, electric motor control systems, and power conversion systems. In John Deere, Dr. Singh won three innovation awards and one collaboration award. He also won the 2020 IEEE Power Electronics Emerging Technology Award and has served as the IEEE Power Electronics Society Distinguished Lecturer (PELS DL) for term 2021-2024 and presently serving as the Chair of PELS DL Program. In 2023, US Department of Energy recognized Dr. Singh's outstanding contributions and insightful technical expertise by Distinguished Achievement Award.

SHORT COURSE

Date: Sunday, May 24, 2026, 8:30-16:30

Venue: MGM Grand Conference Center, 3rd Floor, Chairman's Ballroom Rm 364-369

Short Course Chair: Prof. Victor Veliadis, PowerAmerica/NC State, USA

Time	Title	Speaker
09:00-10:00	Lateral GaN Bi-Directional Switch Technology: Target Applications and New Trends	Dr. Kennith K. Leong
10:00-11:00	Introduction to Silicon Carbide Power Devices: Power MOSFETs and IGBTs	Dr. Sei-Hyung Ryu
11:00-12:00	Advanced Packaging Solutions for Full Exploitation of SiC Power Switches	Prof. Alberto Castellazzi
12:00-13:30	*Lunch (provided)*	
13:30-14:30	How Active Gate Drivers and Power ICs Improve Power Semiconductor Device Performance	Dr. Nicolas Rouger
14:30-15:30	Ultra-Wide-Bandgap Semiconductors for Next-Generation Power Electronics	Dr. Robert Kaplar
15:30-16:30	Gigawatt AI Data Centers: HVDC Power Delivery and Power Semiconductor Needs	Prof. John Shen

SC1. Lateral GaN Bi-Directional Switch Technology: Target Applications and New Trends

Dr. Kennith K. Leong, *Infineon, Austria*

Abstract: For the first time since its introduction at ISPSD 2007, the monolithic GaN bi-directional switch was commercially released last year and adopted in the market. However, much about this new power device is still not widely known or well understood. This presentation will dive into the fundamentals of this innovative class of devices, and their unique characteristics and performance advantages. Furthermore, the presentation will highlight target applications, novel circuit topologies, as well as future market trends enabled by bi-directional switches.

SC2. Introduction to Silicon Carbide Power Devices: Power MOSFETs and IGBTs

Dr. Sei-Hyung Ryu, *Wolfspeed, USA*

Abstract: Wide bandgap properties of Silicon carbide (SiC) make SiC devices very attractive for various power switching applications. SiC power devices have lower conduction and switching losses compared to silicon devices, leading to improved energy efficiency while allowing increased power density of the system. In addition, SiC power devices can operate at significantly higher temperatures than silicon devices without compromising performance, which helps reduce system costs due to lower cooling requirements. The high-performance aspect of SiC power devices makes them desirable for various high power applications, which include renewable energy systems and electric vehicles.

This presentation will provide an overview of various SiC power MOSFET structures, which include planar and trench MOSFETs. A discussion on how SiC power devices differ from silicon devices will be provided. Challenges in SiC power MOSFET optimization for mainstream applications as well as ultra-high voltage applications will be discussed. Advanced structures such as Super Junction MOSFETs and high voltage IGBTs will also be discussed.

SC3. Advanced Packaging Solutions for Full Exploitation of SiC Power Switches

Prof. Alberto Castellazzi, *Kyoto University of Advanced Science, Japan*

Abstract: SiC power MOSFETs have by now become a commercial reality, receiving interest as an alternative to Si IGBTs from application domains as diverse as air conditioning, renewable energies, transportation and industrial machinery. Packaging plays a pivotal role in enabling the full exploitation of the superior characteristics of SiC to yield major and partly disruptive progress in system-level functionality, efficiency, power density and electro-magnetic signature. And the packaging solutions developed over time for Si IGBTs cannot be directly transferred to SiC MOSFETs: innovative bespoke concepts are required. This tutorial will review the operational features of two key switch architectures, half-bridge and bi-directional switches, and discuss modular packaging concepts featuring reduced parasitic capacitance and inductance, high-temperature and high-vibration withstand capability.

SC4. How Active Gate Drivers and Power ICs Improve Power Semiconductor Device Performance

Dr. Nicolas Rouger, *Université de Toulouse, France*

Abstract: New generations of power semiconductor devices are pushing towards higher efficiency, robustness and performance/cost ratio. To make the most from these power devices at system-level, it is essential to understand the close interactions between gate drivers and power

transistors within the power commutation cell. This short course begins by reviewing the state of the art and competing approaches in integrated circuits for gate driver applications. We will then analyze a simple, yet effective, example to highlight both the limitations and opportunities offered by tunable and more flexible gate drivers. Following this introduction, the focus will be on smart gate drivers and their role in improving the performance and reliability of power semiconductor devices, covering key aspects such as active switching control, and the possible benefits of smart gate drivers in power semiconductor design. We will also explore tunability, the challenges of driving parallel devices of the same or complementary technologies, and active control of reverse conduction, all while emphasizing the balance between complexity, performance, and functionality. Finally, the course will conclude by examining how to move beyond traditional trade-offs through releasing some design constraints at the power device level thanks to optimal active gate drivers.

SC5. Ultra-Wide-Bandgap Semiconductors for Next-Generation Power Electronics

Dr. Robert Kaplar, *Sandia National Laboratories, USA*

Abstract: The ultra-wide-bandgap (UWBG) materials such as AlGaN/AlN, Ga2O3, diamond, cubic BN, and others represent the next step in the evolution of semiconductor physics and devices. For power electronics, the anticipated high breakdown electric field of these semiconductors, which is believed to scale roughly with the square of the bandgap, is expected to provide performance advantages over SiC and GaN in much the same way that SiC and GaN have surpassed the performance of Si. However, arguments based on standard metrics such as the Baliga figure of merit are oversimplified, in part due to assumptions that are not satisfied for UWBG materials such as complete ionization of impurity dopants, and a more nuanced analysis is required. This tutorial will provide an overview of the key physical properties of the UWBG semiconductors, and how they contribute to anticipated performance benefits for power electronics based on a more realistic analysis of switch-mode operating conditions. The key challenges associated with the growth and processing of UWBG materials will be presented, such as the quality and availability of suitable substrates, effectively controlling conductivity by impurity doping or other means such as polarization doping, the fabrication of low-resistance ohmic contacts, the synthesis of low-defect-density semiconductor-dielectric interfaces, and bulk and interfacial electronic and thermal transport. The significant progress that has been made over the past several years on these challenges for the primary UWBG semiconductors will be reviewed, and the impact of this progress on practical device structures will be evaluated. Additionally, still-newer emerging UWBG semiconductors will be surveyed. Finally, an overview of the power conversion applications that may motivate the maturation and commercialization of UWBG devices will be given.

SC6. Gigawatt AI Data Centers: HVDC Power Delivery and Power Semiconductor Needs

Prof. John Shen, *Simon Fraser University, BC, Canada*

Abstract: Gigawatt-scale AI data centers are being constructed or planned to meet the ever-increasing demand of Large Language Model (LLM) training and inferencing. DC power is proposed again to replace AC for delivering power from the grid to the GPU racks more efficiently. Nvidia and Open Computing Project (OCP) both advocated 800V HVDC solution in 2025 to address the challenge of power transmission efficiency and limited space for large power cables/busses associated with AC. This new mandate has created new business opportunities for the power electronics and power semiconductor industry. However, the challenges that kept the theoretically advantageous DC power from being adopted into medium- or low-voltage power grids, including 380VDC data centers in the early 2010s remain to be addressed. It is of ultimate importance to provide fault-proof and redundant power to each of the mission-critical GPU rack (~1MW). This talk will review the power distribution architectures, new power electronic blocks, and power semiconductor devices required for a GW HVDC AI data center.

TECHNICAL PROGRAM

Opening Session

Monday, May 25, 2026

Time: 8:30-9:00
Location: Lecture
Chair(s): David Sheridan, *Alpha & Omega Semiconductor*
Sameh Khalil, *Infineon*

Plenary Session

Monday, May 25, 2026

Time: 9:00-10:20
Location: Lecture
Chair(s): Sameh Khalil, *Infineon*
David Sheridan, *Alpha & Omega Semiconductor*

9:00

A0L-A.1 **Power Delivery as the Limiting Factor in AI Systems: From Transistor Scaling to Rack-Scale Power Architecture**
Dr. Ahmed Abou-Alfotouh
AMD, United States

9:40

A0L-A.2 **Power Electronics Systems for Heavy-Duty Off-Road Vehicles**
Dr. Brij Singh
John Deere, United States

Monday, May 25, 2026

A1L-A HV-1: New Power Device Designs and IGBTS

Time: 10:40-12:00
Location: Lecture
Chair(s): Umamaheswara Vemulapati, *Hitachi Energy*
Kota Ohi, *Fuji Electric*

10:40

A1L-A.1 Split-Gate-Resistance-Separation CSTBTTM for Extremely-Low Turn-on Switching Loss, EMI Suppression and High Robustness
Kazuya Konishi[1], Koyo Matsuzaki[1], Kosuke Sakaguchi[2], Ryosuke Kobayashi[2], Masashi Sawada[1], Koutarou Kawahara[1], Shiro Hino[1], Fumihito Masuoka[2]
[1]Advanced Technology R&D Center, Mitsubishi Electric Corporation, Japan; [2]Power Device Works, Mitsubishi Electric Corporation, Japan

11:00

A1L-A.2 Breaking the Eon and Radiated Noise Trade-Off via Deep Split-Gate CSTBT™ with dI/dt Shaping
Kosuke Sakaguchi[1], Kazuya Konishi[2], Ryosuke Kobayashi[1], Gai Fujiki[1], Kazuki Nishida[1], Naoki Ikeda[1], Fumihito Masuoka[1]
[1]Power Device Works, Mitsubishi Electric Corporation, Japan; [2]Advanced Technology R&D Center, Mitsubishi Electric Corporation, Japan

11:20

A1L-A.3 Two Distinct Turn-Off Behavior Variation Mechanisms and CGC Evolution Under Dynamic Avalanche Stress in IGBTs
He Du, Teruyuki Ohashi, Takahiro Kato, Yusuke Kobayashi
Toshiba Corporation, Japan

11:40

A1L-A.4 Cross-Contact Structure for Narrow-Mesa IGBTs: Process Constraint Elimination and Loss-Robustness Balance Optimization
Keisuke Yukawa, Takuya Matsumoto, Shinya Umeki, Takeshi Okamoto, Yuji Ota
ROHM Co., Ltd., Japan

A2L-A SiC-1: SiC Novel Designs and Processes

Time: 13:30-15:10
Location: Lecture
Chair(s): Jeff Joohyung Kim, *Wolfspeed*
Teruyki Ohashi, *Toshiba Electronic Devices & Storage*

13:30

A2L-A.1 A Novel Mesh-Like Variation of Lateral Doping Termination for 4H-SiC Power Devices

Nan Nie[1], Min Ren[1], Xin Zhang[2], Xiao Guo[1], Fang Zheng[2], Anna Zhang[2], Rongyao Ma[2], Siwei Liu[1], Ye Tao[1], Zehong Li[1], Xuan Li[1], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Wuxi China Resources Huajing Microelectronics Co., Ltd., China

13:50

A2L-A.2 First Experimental Demonstration of a Trench-Based Edge-Termination Structure for 1.2 kV SiC MOSFETs

Yoshitaka Kimura[1], Takaaki Tominaga[2], Yutaka Fukui[3], Munenori Ikeda[1], Tomohiro Tamaki[2], Yasuhiro Kagawa[3], Kazushi Kono[1]
[1]Component Production Engineering Center, Mitsubishi Electric Corporation, Japan; [2]Advanced Technology R&D Center, Mitsubishi Electric Corporation, Japan; [3]Power Device Works, Mitsubishi Electric Corporation, Japan

14:10

A2L-A.3 Ultra-High-Voltage 4H-SiC IGBTs Enabled by Wafer Back-Grinding: A Manufacturing Pathway for SiC Bipolar Devices

N. Donato[1], M. Kah[1], F. Udrea[1], G. Gupta[2], M. Pocaterra[2], E. Ceccarelli[2], G. Alfieri[2], B. Boksteen[2], N. Klipfel[2], A. Schöner[3], M. Dinse[4], JH Peters[4], N. Kaminski[4], LA Figueras La Peruta[5], G. Pellegrini[5]
[1]University of Cambridge, United Kingdom; [2]Hitachi Energy, Switzerland; [3]Kista, Sweden; [4]Institute for Electrical Drives, Power Electronics and Devices (IALB), University of Bremen, Germany; [5]Institute of Microelectronics of Barcelona (IMB-CNM-CSIC), Spain

14:30

A2L-A.4 Development of 10.2 mm Square SiC-MOSFET with Lattice-Pattern Deep-p Structure for Electrified Vehicles

Tadashi Misumi, Hidefumi Takaya, Ryuta Arai, Kensuke Hata, Tomohiro Mimura, Keita Hayashi, Naoki Tega, Takahiro Ito, Masaki Konishi
DENSO Corporation, Japan

14:50

A2L-A.5 Novel Self-Aligned Flat Source Contact Architecture for Low On-Resistance SiC Trench MOSFETs

Akifumi Iijima[1], Takaaki Tominaga[1], Shiro Hino[1], Yutaka Fukui[2], Kohei Adachi[2], Hideyuki Hatta[2], Yasuhiro Kagawa[2], Tatsuro Watahiki[1]
[1]Advanced Technology R&D Center, Mitsubishi Electric Corporation, Japan; [2]Power Device Works, Mitsubishi Electric Corporation, Japan

A3L-A GaN-1: Novel GaN Power Devices and Technologies

Time: 15:30-17:10
Location: Lecture
Chair(s): Akira Nakajima, *AIST*
Oliver Hilt, *Ferdinand-Braun-Institut, Berlin*

15:30

A3L-A.1 p-GaN HEMTs with Distributed Drain-Connected p-GaN Islands for Improved In-situ-RDS(on) Stability Under Surge Voltage

Jinggui Zhou[1], Juan Lei[1], Qi Zhou[1,3], Yuqi Liu[1], Yuesi Yu[1], Binju Qiu[1], Yuxi Wan[2], David Zhou[2], Chao Feng[2], Bo Zhang[1]
[1]School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, China; [2]Shenzhen Pinghu Laboratory, China; [3]Institute of Electronic and Information Engineering of UESTC in Guangdong, China

15:50

A3L-A.2 Z-FET：A Low Dynamic RON Normally-OFF AlGaN/GaN HEMT Based on a Multiple Channel Structure

Qinyi Wei[1,2], Qimeng Jiang[3], Xiaotian Tang[1,2], Zhongchen Ji[1,2], Sen Huang[1,2], Xinyu Liu[1,2]
[1]Institute of Microelectronics of the Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China; [3]Southwest Jiaotong University, China

16:10

A3L-A.3 6.2 kV/12.4 mΩ·cm² Superjunction GaN Lateral Field-Effect Rectifier with Low Dynamic ON-Resistance

Junjie Yang[1], Jingjing Yu[1], Jiawei Cui[1], Sihang Liu[1], Hao Chang[1], Han Yang[1], Xuelin Yang[1], Xiaosen Liu[2], Maojun Wang[1], Bo Shen[1], Jin Wei[1]
[1]Peking University, China; [2]Tsinghua University, China

16:30

A3L-A.4 Record-Low RON,SP and RON×QG in Regrowth-Free Low-Voltage p-GaN Gate HEMTs on 200-mm GaN-on-Si Platform

Yan Cheng[1,2], Yu Shi[1,3], David Zhou[1], Xinying Huang[1], Yu Zhang[1], Changan Li[1], Yuhao Wang[1], Zidong Cai[1], Haolin Hu[1], Wei Zeng[1], Zongjie Zhou[2], Yat Hon Ng[2], Xiaoping Wang[1], Chenchang Zhan[3], Yuxi Wan[1], Kevin J. Chen[2]
[1]Shenzhen Pinghu Laboratory, National Center of Technology Innovation for Wide Bandgap Semiconductors (Shenzhen), China; [2]The Hong Kong University of Science and Technology, China; [3]Southern University of Science and Technology, China

16:50

A3L-A.5 Observation and Suppression of Punch-Through Breakdown in Multi-Kilovolt Lateral GaN Superjunction HEMTs

Zineng Yang[1], Yuan Qin[2], Hehe Gong[1], Yuhao Zhang[1]
[1]Center for Advanced Semiconductors and Integrated Circuits and Department of Electrical and Computer Engineering, The University of Hong Kong, China; [2]Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, United States

Tuesday, May 26, 2026

B1L-A LVT-1: Low Voltage Lateral Devices

Time: 8:40-10:00
Location: Lecture
Chair(s): Tanuj Saxena, *Onsemi*
Raffaella Roggero, *STMicro*

8:40

B1L-A.1 Operating Voltage Extension of Fully Isolated nLDMOS Using PBL Junction Engineering and Deep P-Body for Robust E-SOA

Jong-Ho Lee, Hyun-Seok Song, Ji-Hyun Lee, Hye-Won Du, Yong-Keon Choi, Sang Gi Lee
DB HiTek Co., Ltd., Korea

9:00

B1L-A.2 A Novel Split-Channel LDMOS Using Self-Aligned Technology for Low QGD and Short-Channel Effect Suppression in High Frequency DrMOS Application

Dingxiang Ma, Shengjie Qin, Yangjie Liao, Hanwen Bai, Jiawei Wang, Siyuan Lang, Bo Zhang, Ming Qiao
State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Tech. of China, China

9:20

B1L-A.3 Grid-Gate LDMOS Achieving Ultra-Low Specific On-Resistance with Enhanced HCI and Thermal Robustness for DrMOS on a 55nm BCD Platform

Jiawei Wang[1], Ming Qiao[1,2], Siyuan Lang[1], Fanyi Zeng[1], Dingxiang Ma[1], Wenliang Liu[1], Hanwen Bai[1], Yangjie Liao[1], Yifan Wu[1], Shengjie Qin[2], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, China

9:40

B1L-A.4 A Novel Shunt-Triggered SCR with Dual Metal-Bridge for Ultra-High Holding Voltage and Robust ESD Protection

Zhao Qi[1], Jinpeng Hao[1], Yirui Jia[1], Junke Li[1], Fengyu Shi[1], Xuan Li[1], Feng Lin[2], Liang Song[2], Jun Sun[2], Sen Zhang[2], Wenqi Wu[3], Xin Zhang[3], Ming Qiao[1,4], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]CSMC Technologies Corporation, China; [3]Xinhuo Integrated Circuit Industrial Center Co., Ltd., China; [4]Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, China

B2L-A SiC-2: SiC Device Design for Reliability and Ruggedness

Time: 10:20-12:00
Location: Lecture
Chair(s): Ivana Kovacevic, *ETH Zurich*
Shinsuke Harada, *AIST*

10:20

B2L-A.1 Fundamental Device Design Rules of Applying Proton Implantation Technique to SiC MOSFETs for Prevention of the Bipolar Degradation

Naoki Shikama[1], Kazuya Tojima[1], Hideyuki Hatta[1], Hiroki Niwa[2], Hiroyuki Amishiro[2], Katsutoshi Sugawara[2], Yasuhiro Kagawa[1], Tetsuya Nitta[1]
[1]Power Device Works, Mitsubishi Electric Corporation, Japan; [2]Advanced Technology R&D Center, Mitsubishi Electric Corporation, Japan

10:40

B2L-A.2 Enhanced Short-Circuit Robustness in SiC Trench MOSFETs by Dual-JFET Design

Jens Baringhaus, Stephan Schwaiger, Marco Santoro, Alberto Martinez-Limia, Dragos Costachescu, Wolfgang Feiler
Robert Bosch GmbH, Germany

11:00

B2L-A.3 Demonstration of High Single-Event Gate Tolerance in SiC UMOSFET by Trench-Bottom Hole Extraction

Tomoka Suematsu[1], Keisuke Kobayashi[1], Shinichiro Matsunaga[1], Kensuke Takenaka[1], Takeshi Tawara[1], Mitsuo Okamoto[1], Shinsuke Harada[1], Takahiro Suzuki[2], Hiroyuki Shindou[2], Haruka Shimizu[3], Yuki Mori[3], Akio Shima[3], Takahiro Makino[4], Takeshi Ohshima[4]
[3]National Institute of Advanced Industrial Science and Technology, Japan; [2]Japan Aerospace Exploration Agency, Japan; [3]Hitachi, Ltd., Japan; [4]National Institutes for Quantum Science and Technology, Japan

11:20

B2L-A.4 On the SiC/SiO_2 Interface and SiO_2 Gate Reliability of Planar and Trench SiC MOSFETs

P. Moens[1], A. Feng[1], M. Avramenko[1], G. Gomez[1], J. Seo[2], H. Kim[2], D. An[2], S. Maslougkas[3], T. Nigam[4], E. Van Brunt[4]
[1]onsemi, Belgium; [2]onsemi, Korea; [3]onsemi, Sweden; [4]onsemi, United States

11:40

B2L-A.5 A 4H-SiC MOSFET Integrated Trench Diode to Enhance Single-Event Effect Robustness

Yadong Huang[1], Yiru He[1], Maojiu Luo[2], Bo Zhang[1], Yourun Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, China; [2]Gree Electric Appliances, Inc., China

B3L-A ICD: Next Generation Power ICs

Time: 13:30-14:50
Location: Lecture
Chair(s): Jingshu Yu, *Intel*
Makoto Takamiya, *The University of Tokyo*

13:30

B3L-A.1 A Triple-Path Resonant-Tracked Voltage Regulator with Package Inductor for System-on-Wafer Vertical Power Delivery

Renwei Chen, Zhoutong Liu, Xuchen Men, Xuliang Wang, Yan Wang, Xiaosen Liu
Tsinghua University, China

13:50

B3L-A.2 A 700-V Monolithic MOS-Emulated GaN Power IC with Self-Powered Miller Clamping Enabling 70 V/ns CMTI in Resonant Converters

Xinyang Liu[1], Rongxing Lai[1], Fei Teng[1], Xudong Li[1], Wenhong He[1], Wen Xiao[1], Zekun Zhou[1], Bo Zhang[1], Gaofei Tang[2], Wen Shi[2], Zhiwen Dong[2], Qimeng Jiang[2]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]CloudSemi Technology Co., Ltd., China

14:10

B3L-A.3 A Gate Protection Interface Enabling Robust and User-Friendly Gate Driving of GaN/SiC HyFET

Ji Shu[1,2], Mian Tao[3], Yat Hon Ng[1,2], Jiaheng He[1,2], Ziying Li[4], Qingyuan Tang[4], Shi-Wei Ricky Lee[3], Kevin J. Chen[1]
[1]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, China; [2]Hybay Semiconductor Ltd., China; [3]EPACK Lab, The Hong Kong University of Science and Technology, China; [4]Guangdong Fenghua Semiconductor Technology Co., Ltd., China

14:30

B3L-A.4 A 400V GaN Half-Bridge Gate Driver with Self-Protected Fast-Charging Bootstrap and Current Balance Switch Based High-CMTI Level Shifter

Lin-min Chen[1], Chun-wang Zhuang[1], Xin Ming[1], Wei-jia Zhang[2], Nai-long He[3], Sen Zhang[3], Zhi-jiu Wu[1], Yu-ling Sun[1], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, China; [3]Technology Development Department, CSMC Technologies Corporation, China

B4L-A GaN-2: Vertical GaN Power Devices

Time: 14:50-16:10
Location: Lecture
Chair(s): Robert Kaplar, *Sandia National Laboratories*
Lan Wei, *University of Waterloo*

14:50

B4L-A.1 First Experimental Demonstration of Photon-Reabsorption Enhanced Conductivity Modulation in 3 kV/0.18 mΩ·cm² GaN Vertical p-n Diodes

Xinchen Ge[1,2,3], Xiujian Sun[1,2], Xiaolu Guo[2,4], Zhuo Chen[1,2], Chuanjie Li[2], Yaozong Zhong[2], Haoran Qie[2], Meixing Feng[2], Haodong Wang[1,2], Xin Chen[2,4], Hongwei Gao[1,2], Quan Dai[2], Qian Li[2], Yu Zhou[1,2], Shuming Zhang[2], Qian Sun[1,2,4], Hui Yang[1,2,3]
[1]School of Nano-Tech and Nano-Bionics, University of Science and Technology of China (USTC), China; [2]Key Laboratory of Semiconductor Display Materials and Chips, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences (CAS), China; [3]Suzhou Laboratory, China; [4]Guangdong Institute of Semiconductor Micro-Nano Manufacturing Technology, China

15:10

B4L-A.2 Vertical GaN-on-Si MOSFET/JBS-Based Monolithic Bidirectional Switch

Yuchuan Ma[1,2], Changfa Sun[1,2], Yifan Dong[1,2], Ziwei Wang[1,2], Yunsong Xu[3], Maoqing Ling[3], Wen Liu[3], Xiangyu Teng[4], Wei Jia Zhang[4], Chao Liu[1,2]
[1]School of Integrated Circuits, Shandong University, China; [2]Shenzhen Research Institute of Shandong University, China; [3]School of Advanced Tech., Xi'an Jiaotong-Liverpool University, China; [4]Dept. of Electronic and Computer Engineering, Hong Kong University of Science and Technology, China

15:30

B4L-A.3 1.2 kV-Class All Ion-Implanted Vertical GaN-DMOSFETs with Superior Short-Circuit Ruggedness

Nao Suganuma[1], Katsunori Ueno[1], Ryo Tanaka[1], Hirohisa Hirai[2], Akira Nakajima[2], Shinsuke Harada[2], Shinya Takashima[1]
[1]Advanced Technology Laboratory, Fuji Electric Co., Ltd., Japan; [2]Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Japan

15:50

B4L-A.4 Extremely Low On-Resistance AlN-Based SBDs with Distributed Polarization Doping Drift Layer

Issei Sasaki[1], Masanobu Hiroki[2], Kazuaki Ebata[2], Kazuyuki Hirama[2], Yoshitaka Taniyasu[2], Takuya Maeda[1]
[1]University of Tokyo, Japan; [2]NTT Basic Research Laboratories, Japan

B5P-B LVT-P: Low Voltage Power Devices (Poster Session)

Time: 16:30-18:00
Location: Poster
Chair(s): Kuo-Ming Wu, *TSMC*
Lan Wei, *University of Waterloo*

B5P-B.1 90 nm BCD Platform for 5-24V LDMOS with Ultra-Low Specific On-Resistance: Self-Aligned Trimming and Multi-Step Field Plate

Teng Liu[1,2], Yongshun Li[2], Rongshuo Liu[1], Zhenyan Liu[1], Jian Xu[1], Hao Wang[2], Ting Wang[2], Ziao Zhang[2], Huajing Jin[2], Liang Song[2], Nailong He[2], Sen Zhang[2], Ping Li[3], Rongyao Ma[3], Ming Qiao[1], Wentong Zhang[1], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]CSMC Technologies Corporation, China; [3]China Resources Microelectronics, China

B5P-B.2 Seek-BCD: A Domain-Specialized Evolutionary Large Language Model Agent for BCD Technology

Xiaoyun Huang[1], Yixian Song[1], Hongyu Tang[1], Yan Pan[1], Dawei Gao[1,3], Kai Xu[1,2,3]
[1]College of Integrated Circuits, Zhejiang University, China; [2]ZJU-Hangzhou Global Scientific and Technological Innovation Center, China; [3]Zhejiang Technology Innovation Center of CMOS IC Manufacturing Process and Design, China

B5P-B.3 Analysis of Body Diode in Trench Field Plate MOSFETs and Reverse Recovery Charge Reduction by Shrinking the Cell Pitch

Tatsuya Nishiwaki, Seiji Inumiya
Toshiba Electronic Devices & Storage Corporation, Japan

B5P-B.4 Comprehensive Study of Distinct TID Mechanisms in Hardened SGT MOSFET Under On/Off State and Annealing Recovery

Junfeng Yu[1], Jihong Ding[10], Ruihan Gao[1], Haonan Liu[1], Jun Ye[1,3], Xuan Xiao[3,9], Junyan Zhu[1], Chunlei Wu[1], D.W. Zhang[1], Pengcheng Yu[2], Hao Gu[2], Hongping Ma[5], Qingchun Jon Zhang[5], Haiming Xu[4], Tao Wang[4], Qingdong Zhang[4], Liang Li[6], Haiou Li[7], Hong Zhou[8], Jincheng Zhang[8], Xiaofeng Gu[2], Linna Zhao[2], Wei Huang[2]
[1]State Key Laboratory of ASIC & System, College of Integrated Circuits & Micro-Nano Electronics, Fudan University, China; [2]Jiangsu Provincial Key Laboratory of MEMS Sensors and ASIC Manufacturing Technology, School of Integrated Circuits, Jiangnan University, China; [3]Wuxi China Resources Huajing Microelectronics Co., Ltd., China; [4]Wuxi Microelectronics Scientific and Research Center, China; [5]Academy for Engineering & Technology, Fudan

University, China; [6]School of Electronic Information Engineering, Suzhou Vocational University, China; [7]Guilin University of Electronic Technology, China; [8]School of Microelectronics, Xidian University, China; [9]College of Physics, Sichuan University, China; [10]East China Institute of Photo-Electron IC, China

B5P-B.5 Isolation Method for Reducing Current Noise of Hump-Free MOSFET with Extended Active Region in Current Mirror

Kyuyeop Lee, Kyunghan Kim, Dawon Jeong, Jaehyun Yoo, Yonghee Park, Jaehoon Jeong, Yonghoon Kim
Samsung Electronics Co., Ltd., Korea

B5P-B.6 0.15 µm 120 V Si P-epi BCD Technology on Latchup Immunity with Lowest Ron nLDMOS, HV ESD of Combined PNP Structure for Automotive Application

Feng Qiu[1,3], Xiaodong Yang[1], Zhuang Wang[1], Shijie Wang[1], Fengsong Liu[1,3], Linhui Hu[1,3], Liming Liao[3], Qiang Zhang[3], Hongtao Jiang[3], Pengcheng Yu[2], Hao Gu[2], Shijin Ding[1], Chunlei Wu[1], D.W. Zhang[1], Haiou Li[4], Hong Zhou[5], Jincheng Zhang[5], Linna Zhao[2], Xiaofeng Gu[2], Wei Huang[2]
[1]State Key Laboratory of Integrated Chips and Systems, College of Integrated Circuits and Micro-Nano Electronics, Fudan University, China; [2]Jiangsu Provincial Key Laboratory of MEMS Sensors and ASIC Manufacturing Technology, School of Integrated Circuits, Jiangnan University, China; [3]Shanghai GTA Semiconductor Co., Ltd., China; [4]Guangxi Key Laboratory of Precision Navigation Technology and Applications, Guilin University of Electronic Technology, China; [5]School of Microelectronics, Xidian University, China

B5P-B.7 Energy Band Analysis of Injected and Trapped Charge in Shield Oxide: Effects on Electric Field and Breakdown Behavior in Power Trench MOSFETs

Zeinab Ramezani, Mohammad Tanvir Quddus, Ziyi Wang, Prasad Venkatraman
onsemi, United States

B5P-B.8 A Novel Notched-Gate LDMOS for Robust Reliability via Electric Field Modulation and Low Gate Charge on 55-nm BCD Platform

Dingxiang Ma, Hanwen Bai, Fanyi Zeng, Jiawei Wang, Yangjie Liao, Bo Zhang, Ming Qiao
State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China

B5P-B.9 Degradation of Unclamped Inductive Switching (UIS) Capability Due to Gate Oxide Breakdown and Mitigation Through Layout Optimization in Split-Gate Trench MOSFETs

Keita Aoyama, Casey Clendennen, Shinichiro Hisano, Hajime Kataoka, Shinpei Onishi, Tomoaki Shinoda
ROHM Co., Ltd., Japan

B5P-B.10 Experimental Demonstration of a Novel Double-Gate LDMOS with Optimized Conduction and Switching Losses Based on a 55nm BCD Platform

Jiawei Wang[1], Ming Qiao[1,2], Hanwen Bai[1], Fanyi Zeng[1], Shuting Huang[1], Siyuan Lang[1], Dingxiang Ma[1], Kefei Ma[1], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, China

B5P-C ICD-P: Power IC Design (Poster Session)

Time: 16:30-18:00
Location: Poster
Chair(s): Kuo-Ming Wu, *TSMC*
Roy King-Yuen Wong, *National Tsing Hua University*

B5P-C.1 A 48V 93.7%-Peak-Efficiency Dual-Edge Soft-Switching GaN Boost Converter with Adaptive Pulse Stabilizer for LiDAR Transmitter Achieving 0.48ns Pulse Width and 5.6ns Propagation Delay

Yi Fang[1], Bin Chen[1], Longcheng Pi[1], Yike Fang[1], Yuhang Zheng[1], Jingni Hong[1], Jianlong Lin[2], Xiaopeng Yu[1], Xugang Ke[1]
[1]Zhejiang University, China; [2]Primechip Semiconductor, China

B5P-C.2 A GaN Device with Self-Generated Negative Voltage for Enhanced Turn-Off Reliability

Xinyang Liu[1], Rongxing Lai[1], Yun Dai[1], Xudong Li[1], Wen Xiao[1], Wenhong He[1], Zekun Zhou[1], Bo Zhang[1], Gaofei Tang[2], Wen Shi[2], Zhiwen Dong[2], Qimeng Jiang[2]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]CloudSemi Technology Company Ltd., China

B5P-C.3 First Demonstration of Cryogenic Power Converter Operational at 4 Kelvin Using GaN Power IC

Xin Yang[1], Liyang Jin[2], Bixuan Wang[3], Ricardo Garcia[4], Han Wang[1], Liyan Zhu[3], Shengke Zhang[4], Linbo Shao[2], Yuhao Zhang[1]

[1]Center for Advanced Semiconductors and Integrated Circuits and Department of Electrical and Computer Engineering, The University of Hong Kong, China; [2]Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, United States; [3]Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, United States; [4]Efficient Power Conversion Corporation, United States

B5P-C.4 A High-Temperature Three-Phase Silicon Carbide MOSFET Power Module with Integrated Low Propagation and High Noise Immunity Gate Driver

Qianheng Dong[1], Jing Zhu[2], Yifei Zheng[1], Bowen Xue[1], Xiang Fan[1], Siyang Liu[1], Long Yuan[3], Weifeng Sun[1]

[1]National ASIC System Engineering Research Center, Southeast University, China; [2]Wuxi Institute of Integrated Circuit Technology, Southeast University, China; [3]State Key Laboratory of Wide-Bandgap Semiconductor Devices and Integrated Technology, China

B5P-C.5 Monolithic GaN Digital Integrated Circuits for Ultrawide Temperature Range from 5 K to 800 K

Ang Li[1,2,3], Yunsong Xu[1,3], Wen Liu[1,3], Guohao Yu[2], Baoshun Zhang[2]

[1]School of Advanced Technology, Xi'an Jiaotong-Liverpool University, China; [2]Nanofabrication Facility, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences (CAS), China; [3]Advanced Semiconductor Research Center, Xi'an Jiaotong-Liverpool University, China

B5P-D GaN-P1: GaN Devices (Poster Session)

Time: 16:30-18:00
Location: Poster
Chair(s): Ayanori Gatto, *Mitsubishi Electric*
Lan Wei, *University of Waterloo*

B5P-D.1 Difference in Overvoltage Stress Behavior Between CIS and UIS in Ohmic p-Gate GaN HEMTs

Wataru Saito, Shin-ichi Nishizawa
Kyushu University, Japan

B5P-D.2 Impact of Integrated Substrate Potential Control (SPC) Circuits and Dual Field-Plates on Dynamic ON-Resistance in GaN Monolithic Bidirectional Switches

Junsong Jiang[1], Gang Liu[1], Zhiwen Dong[2], Yao Chen[1], Hongfeng Chen[1], Xin Chu[1], Fengping Lin[1], Xingang Ren[1], Gaofei Tang[2], Xi Tang[1]
[1]Anhui University, China; [2]CloudSemi Tech. Co., Ltd., China

B5P-D.3 Bidirectional Gate-to-Source ESD Protection Circuit with Adjustable Turn-on Voltage for GaN-on-Silicon Power HEMT

Chieh-Chen Ker[1], Chun-Yu Lin[1], Ming-Dou Ker[1], Hung-Jen Chen[2], Yong-Fen Hsieh[2]
[1]National Yang Ming Chiao Tung University, Taiwan; [2]Materials Analysis Technology Inc., Taiwan

B5P-D.4 Enhanced Dynamic V_{TH} Stability by Inserting a Hole Release Path in the Barrier for Normally off HEMTs with Regrown p-GaN Gate

Hongwei Gao[1,2], Yaozong Zhong[1,2], Yifan Dong[1,2], Xin Chen[1,2,3], Haodong Wang[1,2], Haoran Qie[2], Xiaolu Guo[1,2], Jianxun Liu[1,2], Wenwen Li[1,2], Meixing Feng[1,2], Qian Sun[1,2], Hui Yang[2]
[1]School of Nano Tech. & Nano Bionics, University of Science & Tech. of China, China; [2]Key Lab of Semiconductor Display Materials & Chips, Suzhou Institute of Nano-Tech & Nano-Bionics, Chinese Academy of Sciences, China; [3]Guangdong Institute of Semiconductor Micro-nano Mfg. Tech., China

B5P-D.5 650-V All-GaN Cascode Device Featuring Stacked Packaging and Flux-Cancellation Layout for Concurrent Minimization of Parasitic L/C

Yunheng Hu[1], Lingyan Shen[1], Xuetong Zhou[1], Long Chen[2], Li Zheng[1], Xinhong Cheng[1]
[1]Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, China; [2]Guangdong Ziener Technology Company Ltd, China

B5P-D.6 Demonstration of E-Mode GaN Monolithic Bidirectional Switch Based on Gate Oxygen Plasma Treatment with Blocking Voltage Over 2.9 kV

Zifeng Qu[1,2], Jiachen Duan[1,2], Ang Li[3], Xuanming Zhang[1,2], Yunsong Xu[1,2], Hao Tian[1,2], Yizhou Jiang[1,2], Guohao Yu[3], Chao Long[2], Wen Liu[1,2], Huiqing Wen[1,2]
[1]School of Advanced Technology, Xi'an Jiaotong-Liverpool University, China; [2]Department of Electrical Engineering and Electronics, University of Liverpool, United Kingdom; [3]Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, China

B5P-D.7 1.4kV/1.61mΩ·cm² Vertical p-NiO/n-GaN Heterojunction Diodes with Deep Helium-Implanted Edge Termination and Oxygen Plasma Treatment

Zihao Huang[1], Huile Zhang[1], Jiajun Han[2], Kangkai Fan[1], Yu Xu[1], Yutong Wu[1], Fan Yang[1], Chunyan Chen[1], Hezhou Liu[1], Jun He[1], Junfa Mao[1], Xinke Liu[1]
[1]Shenzhen University, China; [2]South China Normal University, China

B5P-D.8 3.5 kV, 8.9 mΩ·cm² Enhancement-Mode GaN Superjunction Monolithic Bidirectional Switch

Zifeng Qu[1,2], Jiachen Duan[1,2], Ang Li[3], Hao Tian[1,2], Yunsong Xu[1,2], Xuanming Zhang[1,2], Yizhou Jiang[1,2], Guohao Yu[3], Chao Long[2], Wen Liu[1,2], Huiqing Wen[1,2]
[1]School of Advanced Technology, Xi'an Jiaotong-Liverpool University, China; [2]Department of Electrical Engineering and Electronics, University of Liverpool, United Kingdom; [3]Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, China

B5P-D.9 Wafer-Scale N-Polar GaN-on-SiC by Direct Bonding Epitaxial Layer Transfer for HEMTs

Bohan Guo[1,2,3], Guohao Yu[2,3], Jiaan Zhou[2,3], Ang Li[2,3], Runxian Xing[2,3], An Yang[1,2,3], Yifan Yan[1,2,3], Ziqi Zheng[1,2,3], Kai Cheng[4], Jianping Liu[1,2,3], Zhongming Zeng[1,2,3], Baoshun Zhang[1,2,3]
[1]Department of Nano-Tech and Nano-Bionics, University of Science and Technology of China, China; [2]Department of Nano Science and Nano Technology Institute, University of Science and Technology of China, China; [3]Department of Nanofabrication Facility, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, China; [4]Enkris Semiconductor Inc., China

B5P-D.10 GaN Monolithic Bidirectional Switch (MBDS) with Substrate Control Circuit and its Application in Bridgeless-Boost PFC Converter

Hao Chang[1], Yunhong Lao[1], Yinwen Tang[2], Hu Zhou[2], Peixuan Wang[1], Qianzhu Li[1], Junjie Yang[1], Jiawei Cui[1], Maojun Wang[1], Bo Shen[3], Gaofei Tang[2], Jin Wei[1]
[1]School of Integrated Circuits, Peking University, China; [2]CloudSemi Technology Company Ltd., China; [3]School of Physics, Peking University, China

B5P-D.11 Extended Gate-ESD Analysis in p-GaN Power HEMTs: Forward-ESD Impact of Top/Bottom AlGaN Spacers with Variant Al Composition and Reverse-ESD Engineering via Field Plates

Po-Yen Huang[1], Haoran Wang[2], Chun-Hao Lai[2], Wei-Ting Hsu[2], Chang-Jui Tu[2], Xi Jie Lim[2], Shawn S. H. Hsu[1,2], Benoit Bakeroot[3,4], Matteo Borga[3], Niels Posthuma[3], Roy K.-Y. Wong[1,2]

[1]College of Semiconductor Research, National Tsing Hua University, Taiwan; [2]Institute of Electronics Engineering, National Tsing Hua University, Taiwan; [3]imec, Belgium; [4]CMST, imec and Ghent University, Belgium

B5P-D.12 Investigations of CMOS-Compatible 1200 V E-Mode p-GaN Gate HEMTs on 8-Inch Si Substrate with Thick (>8 µm) Epitaxial Layer

Hui Jiao[1,2], Chao Feng[1], Zidong Cai[1], Danfeng Mao[1], Junye Wu[1], Yitian Gu[1], Rongxin Du[1], Haolin Hu[1], Wei Zeng[1], Qing Wang[3], Hongyu Yu[4], David Zhou[1], Yuxi Wan[1]

[1]Shenzhen Pinghu Laboratory, China; [2]National Graduate College for Engineers, Southern University of Science and Technology, China; [3]School of Microelectronics, Southern University of Science and Technology, China; [4]School of Integrated Circuit, Shenzhen Polytechnic University, China

B5P-D.13 Enhanced Robustness Against Hot-Electron-Induced Degradation in Selective Epitaxial p-GaN Gate HEMTs Enabled by Thick AlGaN Barriers

Haohao Chen[1], Jinjin Tang[1], Junting Chen[1], Jianxun Liu[2], Siyuan Ye[1], Sijiang Wu[1], Zhaojun Liu[1], Qian Sun[2], Mengyuan Hua[1]

[1]Department of Electronic and Electrical Engineering, Southern University of Science and Technology, China; [2]Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, China

B5P-D.14 A Monolithically-Integrable Series-RC Damping Concept for GaN HEMTs Validated by Board-Level Emulation in Double-Pulse Tests

Heng Zhang[1], Zhuocheng Wang[1], Fangzhou Wang[1], P. Xing[1], Chao Liu[1], Ruize Sun[1,2], Wanjun Chen[1,2], Bo Zhang[1]

[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Institute of Electronic and Information Engineering of UESTC in Guangdong, China

B5P-D.15 100-nm-Wfin E-Mode GaN Tri-Gate HEMT with 1.87 GW/cm² Baliga Figure-of-Merit

Yu Li[1,2], Haochen Zhang[2], Guohao Yu[1,2], Ang Li[2], Gaofu Guo[2], Tiwei Chen[2], Liying Ding[2], Tiantian Deng[2], Jiawei Ye[2], Yong Cai[1,2], Zhongming Zeng[1,2], Baoshun Zhang[1,2]
[1]School of Nano-Tech and Nano-Bionics, University of Science and Technology of China, China; [2]Nanofabrication Facility, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences (CAS), China

B5P-D.16 Bowtie p-GaN HEMT Source Follower Featuring 6 – 45V Wide Input Range and 1.48 MHz Operation with Monolithic Integrated Common-Source Amplifier for Bandwidth Extension in HV Current Sense Application

P.-S. Kuo[1], C. Langpoklakpam[1], Y.-C. Wang[2], H.-L. Chiang[1], C. Sung[1], P.-T. Chen[1], W.-C. Lin[1], S. Elangovan[3], C.-L. Hung[3], Y.-K. Hsiao[3], H.-C. Kuo[1,3], C.-C. Tu[1,2,3], T.-L. Wu[1]
[1]National Yang Ming Chiao Tung University, Taiwan; [2]National Central University, Taiwan; [3]Hon Hai Research Institute, Taiwan

B5P-D.17 Demonstration of 10 a Switching of Vertical GaN p–n Diodes with Mesa-Free Termination Structure

Yoshinao Miura, Hirohisa Hirai, Akira Nakajima, Shinsuke Harada
National Institute of Advanced Industrial Science and Technology, Japan

B5P-D.18 High Thermal Stability of Threshold Voltage in p-Cr_2O_3 Gated AlGaN/GaN HEMTs

Jingang Li[1,2], Hao Tian[1,2], Maoqing Ling[1,2], Jiachen Duan[1,2], Zifeng Qu[1,2], Ye Liang[1,2], Harm van Zalinge[2], Ivona Z. Mitrovic[2], Ping Zhang[1,2], Kain Lu Low[1,2], Sen Huang[3], Wen Liu[1,2]
[1]School of Advanced Technology, Xi'an Jiaotong-Liverpool University, China; [2]Department of Electrical Engineering and Electronics, University of Liverpool, United Kingdom; [3]Institute of Microelectronics, University of Chinese Academy of Sciences, China

B5P-E Ga2O3 and Diamond-P: Ga2O3 and Diamond (Poster Session)

Time: 16:30-18:00
Location: Poster
Chair(s): Ayanori Gatto, *Mitsubishi Electric*
Roy King-Yuen Wong, *National Tsing Hua University*

B5P-E.1 High-Voltage Ga_2O_3 Schottky Barrier Diodes with Inserted Semi-Insulating Microcolumns for Suppression of Reverse Current

Chunyan Chen, Jiachang Guo, Xue Fan, Huile Zhang, Kangkai Fan, Yu Xu, Zihao Huang, Yiyang Li, Bo Wang, Jun He, Junfa Mao, Xinke Liu
Shenzhen University, China

B5P-E.2 High-Performance and Reliability-Enhanced β-Ga_2O_3 Trench Schottky Barrier Diodes with Ion-Implantation Shielding Layer

Ming Li[1], Zhang Wen[1], Zugui Jiang[1], Songquan Yang[1], Bangyao Mao[2], Weizhe Bi[1], Leidang Zhou[1], Mingchao Yang[1], Yue Hao[2], Li Geng[1]
[1]Xi'an Jiaotong University, China; [2]Xidian University, China

B5P-E.3 Device Design Insights for Ga_2O_3 SBDs from System-Level Thermal and Power Loss Analysis

Haoran Wang, Po-Yen Huang, Ang Lee, Shawn S. H. Hsu, Roy K.-Y. Wong
National Tsing Hua University, Taiwan

B5P-E.4 Combined Degradation Mechanism of Leakage-Temperature of Highly Doped Epitaxial β-Ga_2O_3 SBDs During 5 MeV Proton Irradiation

Jiao Liang[1], Wenzhang Du[2], Yuangang Wang[3], Xinbo Zou[4], Yiwu Qiu[5], Xinjie Zhou[5], Hao Gu[9], Pengcheng Yu[9], Zhihong Feng[3], Hongping Ma[1], Qingchun Jon Zhang[1], Hong Zhou[6], Jincheng Zhang[6], Haiou Li[7], Zhuorui Tang[8], Junfeng Yu[2], Junyan Zhu[2], Chunlei Wu[2], D.W Zhang[2], Wei Huang[9]
[1]Institute of Wide Bandgap Semiconductors and Future Lighting, College of Intelligent Robotics and Advanced Manufacturing, Fudan University, China; [2]State Key Laboratory of Integrated Chips and Systems, College of Integrated Circuits and Micro-Nano Electronics, Fudan University, China; [3]National Key Laboratory of ASIC, Hebei Semiconductor Research Institute, China; [4]School of Information Science and Technology (SIST), ShanghaiTech University, China; [5]Wuxi Microelectronics Scientific and Research Center, China; [6]School of Microelectronics, Xidian University, China; [7]Guangxi Key Laboratory of Precision Navigation Technology and Applications, Guilin University

of Electronic Technology, China; [8]School of Electronic and Information Engineering, Foshan University, China; [9]Jiangsu Provincial Key Laboratory of MEMS Sensors and ASIC Manufacturing Technology, School of Integrated Circuits, Jiangnan University, China

B5P-E.5 A Novel Electric Field Modulation Ga_2O_3 Schottky Barrier Diode with Nitrogen-Ion Implantation Combine with Trench Field Limit Rings and Floating Metal Rings Termination

Moufu Kong[1], Mingliang Yang[1], Gaofu Guo[2], Jiaxin Li[1], Liang Zhao[1], Xiaodong Zhang[2]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Nanofabrication Facility, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, China

B5P-E.6 Demonstration of β-Ga_2O_3 Lateral Heterojunction Diodes with 450 V Single-Event Burnout Voltage

Song He[1], Jinyang Liu[1], Guangwei Xu[1], Ziyuan Wang[1], Weibing Hao[1], Da Yu[1], Tianqi Wang[2], Jie Luo[3], Jie Liu[3], Xuanze Zhou[1], Shu Yang[1], Shibing Long[1]
[1]School of Microelectronics, University of Science and Technology of China, China; [2]Harbin Institute of Technology, China; [3]Institute of Modern Physics, Chinese Academy of Sciences, China

B5P-E.7 Internal Field Optimization Using a Localized Bottom SiO_2 in Vertical β-Ga_2O_3 FinFETs

Gaofu Guo[1,2], Anjing Luo[1], Tiwei Chen[1], Zhucheng Li[1], Yu Li[1], Dengrui Zhao[1,2], Yi Li[2], Li Zhang[1], Chunhong Zeng[1], X. Zhang[1], Zhongming Zeng[1], Xianqi Dai[2], Baoshun Zhang[1]
[1]Nanofabrication Facility, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences (CAS), China; [2]School of Physics, Henan Normal University, China

B5P-E.8 Enhanced On-State Performance of Vertical β-Ga_2O_3 UMOSFETs via MOCVD-Grown Sidewall Regrown Channels

Anjing Luo[1,2], Zhucheng Li[1,2], Gaofu Guo[2], Xuanze Zhou[3], Tiwei Chen[2], Li Zhang[2], Guangwei Xu[3], Chunhong Zeng[1,2], Xiaodong Zhang[1,2], Shibing Long[3], Zhongming Zeng[1,2], Baoshun Zhang[1,2]
[1]School of Nano-Technology and Nano-Bionics, University of Science and Technology of China, China; [2]Nanofabrication Facility, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences (CAS), China; [3]School of Microelectronics, University of Science and Technology of China, China

B5P-E.9 Investigation of Bias Temperature Instability in β-Ga_2O_3 UMOSFET with N-Ion Implanted Current Blocking Layers
Xuanze Zhou, Qi Liu, Xiang Li, Huidong Yao, Shu Yang, Guangwei Xu, Shibing Long
University of Science and Technology of China, China

B5P-E.10 1.36 kV Planar-Gate Ga_2O_3 Cavet with Nitrogen-Graded Multi-Implanted Current Blocking Layer
Jiahao Yao[1,2], Hehe Gong[3], Gaofu Guo[2], Anjing Luo[2], Fang-Fang Ren[1], Shulin Gu[1], Rong Zhang[1], Yuhao Zhang[3], Xiaodong Zhang[2], Jiandong Ye[1]
[1]School of Electronic Science and Engineering, Nanjing University, China; [2]Nanofabrication Facility, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences (CAS), China; [3]Department of Electrical and Electronic Engineering, The University of Hong Kong, China

B5P-E.11 Demonstration of Breakdown Voltage Enhancement in HfO_2 Normally-Off Diamond FETs via Source Field Plate
Junhou Cao[1], Xinyu Zhou[1], Lei Huang[1], Tuanzhuang Wu[1], Zhaoxiang Wei[1], Xiangrui Fan[1], Yiren Yu[1], Xinxin Yu[2], Sheng Li[1], Ran Ye[1], Jie Ma[1], Long Zhang[1], Jiaxing Wei[1], Siyang Liu[1], Weifeng Sun[1]
[1]National ASIC System Engineering Research Center, Southeast University, China; [2]CETC Key Laboratory of Carbon-Based Electronics, Nanjing Electronic Devices Institute, China

Wednesday, May 27, 2026

C1L-A HV-2: High Voltage Power Devices
Time: 8:40-10:00
Location: Lecture
Chair(s): Craig Fisher, *Vishay*
Yusuke Yamashita, *Toyota Central R&D Labs*

8:40
C1L-A.1 Potential of Sb-Doped MCZ Wafer for 300-mm Si-Based High Voltage Power Devices Rating Up to 6.5kV
Katsumi Nakamura, Yosuke Nakanishi
Power Device Works, Mitsubishi Electric Corporation, Japan

9:00
C1L-A.2 Novel Equivalent Simulation Method and Experimental Zero Failure Verification of Optimized 650V SJ MOSFETs Under 100% Rated Voltage HTRB
Daoming Shen, Hongyan Ge, Jie Zhang, Bo Zhang, Ming Qiao
State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China

9:20

C1L-A.3 Demonstration of 1200V SOI PLDMOS with Optimized Substrate P-sub/DN Junction for High Saturation Current

Zheng Zhang[1], Chengwu Pan[1], Mengyan Wu[1], Jiayu Li[1], Yuncong Li[1], Nailong He[2], Dejin Wang[2], Sen Zhang[2], Siyang Liu[1], Jie Ma[1], Weifeng Sun[1], Long Zhang[1]
[1]National ASIC System Engineering Research Center, Southeast University, China; [2]CSMC Technologies Corporation, China

9:40

C1L-A.4 Device Structure Estimation by Inverse Calculation and its Application to Semiconductor Manufacturing

Tomohiko Mori[1], Ryosuke Okachi[1], Junya Muramatsu[1], Makoto Kuwahara[1], Daigo Kikuta[1], Takaaki Aoki[2], Satoshi Kojima[2], Fumitaka Kato[2], Takafumi Arakawa[2]
[1]Toyota Central R&D Labs., Inc., Japan; [2]DENSO Corp., Japan

C2L-A Ga2O3: Ultra Wide Bandgap Devices

Time: 10:20-12:00
Location: Lecture
Chair(s): Kung-Yen Lee, *National Taiwan University*
Alexander Bolotnikov, *Onsemi*

10:20

C2L-A.1 Over 3.5 kV (011) β-Ga_2O_3 Schottky Barrier Diode and First Demonstration of 4.7 kV NiO-Based (011) β-Ga_2O_3 Heterojunction Diode

Junpeng Wen, Jinyang Liu, Qiuyan Li, Lequan Wang, Yuanjie Ding, Song He, Xuanze Zhou, Shu Yang, Guangwei Xu, Shibing Long
University of Science and Technology of China, China

10:40

C2L-A.2 Over 2.5 GW/cm^2 Vertical β-Ga_2O_3 Schottky Barrier Diode with High-K Field Plate and Multi-Zone Gradient Rings Assisted JTE

Lequan Wang[1], Jinyang Liu[1], Song He[1], Junpeng Wen[1], Qiuyan Li[1], Yuanjie Ding[1], Weibing Hao[2], Xuanze Zhou[1], Shu Yang[1], Guangwei Xu[1], Shibing Long[1]
[1]University of Science and Technology of China, China; [2]National University of Singapore, Singapore

11:00

C2L-A.3 0.79 mΩ·cm^2 and 1.1 kV Vertical Mo/β-Ga_2O_3 Deep-Trench-HJBS Diode with Double Drift Layers

Qiuyan Li[1], Jinyang Liu[1], Qi Liu[1], Song He[1], Zaitian Han[1], Junpeng Wen[1], Lequan Wang[1], Weibing Hao[2], Xuanze Zhou[1], Qin Hu[1], Shu Yang[1], Guangwei Xu[1], Shibing Long[1]
[1]University of Science and Technology of China, China; [2]National University of Singapore, Singapore

11:20

C2L-A.4 Area Scaling-Up of β-Ga_2O_3 Schottky Barrier Diodes Achieving 62 A Surge Current and 1.9 kV Breakdown Voltage

Jinyang Liu, Qiuyan Li, Xuanze Zhou, Shu Yang, Zheyang Zheng, Qin Hu, Guangwei Xu, Shibing Long
University of Science and Technology of China, China

11:40

C2L-A.5 Single-Event Effects and Corresponding Nanoscale Microstructure in β-Ga_2O_3 UMOSFETs: Device Reliability and Failure Mechanism

Da Yu[1], Huidong Yao[1], Xuanze Zhou[1], Qi Liu[1], Song He[1], Xuan Xie[1], Tianqi Wang[2], Lei Shu[3], Guangwei Xu[1], Shu Yang[1], Bo Li[3], Shibing Long[1]
[1]School of Microelectronics, University of Science and Tech. of China, China; [2]Harbin Institute of Tech., China; [3]Institute of Microelectronics, Chinese Academy of Sciences, China

C3L-A PK: Module and Packaging Technologies

Time: 13:30-15:10
Location: Lecture
Chair(s): Emre Gurpinar, *Joby Aviation*
Weijia Zhang, *Hong Kong University*

13:30

C3L-A.1 Vertical Power Delivery for 5 kW AI Systems: From Advanced Passives to GaN IC Integration

Jingshu Yu, Nicolas Butzen, Harish K. Krishnamurthy, Samuel Bader, James Waldemer, Jagar Singh, Kaladhar Radhakrishnan, Huong T. Do, Mausamjeet Khatua, Minxiang Gong, Sheldon Weng, Zakir K. Ahmed, Suhwan Kim, Krishnan Ravichandran, Heli Vora, Prafful Golani, Pratik Koirala, Michael Beumer, Ahmad Zubair, Han Wui Then
Intel Corporation, United States

13:50

C3L-A.2 High Power Density SiC Power Module Enabled by a Multi-Functional Si Chip

Hideo Komo[1], Michael Rogers[1], Makoto Ueno[2], Kazuhiro Nishimura[3], Noboru Morimoto[3], Shinsuke Godo[3]
[1]Power Device Works, Mitsubishi Electric Corporation, United States; [2]Melco Semiconductor Engineering Corp., Japan; [3]Power Device Works, Mitsubishi Electric Corporation, Japan

14:10

C3L-A.3 A Hybrid-Package 3-D GaN Power Module with Optimal Thermal Performance and High-Density Integration

Haobin Wei[1], Shenglei Zhao[1], Xiaoqing Liu[1], Fugang Huang[2], Shuang Liu[2], Qiao Du[1], Xuejing Sun[1], Longyang Yu[1], Ming Xiao[1], Shuzhen You[1], Yue Hao[1], Jincheng Zhang[1]
[1]State Key Laboratory of Wide Bandgap Semiconductor Devices and Integrated Technology, Xidian University, China; [2]Sichuan Provincial Engineering Research Center of High Efficiency Power Converter Technology, China

14:30

C3L-A.4 Surge Capability of SiC MOSFETs in the Third Quadrant: Impact of Advanced Packaging Structures

Binqi Liang[1], Feilin Zheng[1], Hao Li[2], Xuebao Li[1], Rui Jin[2], Xiang Cui[1]
[1]North China Electric Power University, China; [2]Beijing Institute of Smart Energy, Huairou Laboratory, China

14:50

C3L-A.5 Electroplated Copper as Front-Side Source Metal for Enhanced Electrical Performance and Reliability of 1200 V Planar SiC MOSFETs

Cen Tang[1], Hongsheng Yi[1], Junyou Wang[1], Yuehua Hong[1], Longgu Tang[1], Wei Lu[1], Wentao Yang[1], Jin Rao[1], Hamada Kimimori[2]
[1]Huawei Technologies Co., Ltd., China; [2]Huawei Technologies Japan K.K., Japan

C4P-B HV-P: High Voltage Devices (Poster Session)

Time: 15:30-17:00
Location: Poster
Chair(s): Ayanori Gatto, *Mitsubishi Electric*
Fisher Craig, *Vishay*

C4P-B.1 A Novel Trench IGBT with Floating P-Region Controlled Split Gate for Low EMI Noise

Tongyang Wang[1], Zehong Li[1,2], Xuan Wang[1,2], Ziming Xia[1], Yige Zheng[1], Zhaoqing Jin[1], Min Ren[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Chongqing Institute of Microelectronics Industry Technology, University of Electronic Science and Technology of China, China

C4P-B.2 Experimental Demonstration of Superjunction MOSFET with Low-Barrier NPN Transistor for Low Reverse Recovery Charge

Tongyang Wang[1], Zehong Li[1,2], Xuan Wang[1,2], Ziming Xia[1], Yige Zheng[1], Zhaoqing Jin[1], Min Ren[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Chongqing Institute of Microelectronics Industry Technology, University of Electronic Science and Technology of China, China

C4P-B.3 Novel Gate-Controlled Soft Turn-Off Technique for Short-Circuit Protection in Double-Gate IGBTs

Teruyuki Ohashi[1], He Du[1], Satoshi Yoshida[1], Keigo Arita[1], Yusuke Hayashi[1], Tomoko Matsudai[2], Yusuke Kobayashi[1]
[1]Corporate Laboratory, Toshiba Corporation, Japan; [2]Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage Corporation, Japan

C4P-B.4 Deep Split-Dummy-Active CSTBT™ Enabling Simultaneous VCE(sat) and EON Reduction

Reona Furukawa[1], Kazuya Konishi[2], Takashi Fujimoto[1], Fumihito Masuoka[1]
[1]Power Device Works, Mitsubishi Electric Corporation, Japan; [2]Advanced Technology R&D Center, Mitsubishi Electric Corporation, Japan

C4P-B.5 Multi-Gate Control for Conduction Loss Reduction via Transient Built-in Voltage Bypass in IGBT

Takato Yamamoto[1], Yusuke Kobayashi[1], Tomoko Matsudai[2], Ryohei Gejo[2], Kota Kato[2], Tatsunori Sakano[1], Teruyuki Ohashi[1], Munetoshi Fukui[3], Takuya Saraya[3], Kazuo Itou[3], Toshihiko Takakura[3], Shinichi Suzuki[3], Toshiro Hiramoto[3]
[1]Toshiba Corporation, Japan; [2]Toshiba Electronic Devices & Storage Corporation, Japan; [3]University of Tokyo, Japan

C4P-B.6 In-Situ Characterization Method for Current Distribution in Press-Pack IGCT Based on Active Avalanche Mechanism

Fucheng Liu[1,2], Jiapeng Liu[1], Songwei Li[2], Jiabin Wang[1], Chunpin Ren[1], Xiaozhao Li[2], Hui Liu[2], Xiaoguang Wei[2], Jinpeng Wu[1,2]
[1]Department of Electrical Engineering, Tsinghua University, China; [2]Next Generation Power System Research Center, Huairou Laboratory, China

C4P-B.7 A Device-Capacitance-Controlled LC Oscillation Suppression in Split-Gate CSTBT™ Based on Barkhausen Stability Analysis
Kazuki Nishida[1], Naoki Ikeda[1], Kosuke Sakaguchi[1], Ryosuke Kobayashi[1], Kazuya Konishi[2], Rei Yoneyama[1]
[1]Power Device Works, Mitsubishi Electric Corporation, Japan; [2]Advanced Technology R&D Center, Mitsubishi Electric Corporation, Japan

C4P-B.8 Experimental Demonstration of Reduced Bulk Field Mechanism in 800 V LDMOS via a Novel Deep-Trench Sidewall Protection Implantation Technology
Jian Xu[1], Teng Liu[1,2], Yueyu Zhang[1], Zhenyan Liu[1], Yiduo Xie[1], Longhui Lin[1], Qiaofeng Lin[1], Yongsheng Sun[3], Hao Fang[3], Xiaofeng Lai[1], Jiawei Wang[1], Hao Wang[2], Ting Wang[2], Ziao Zhang[2], Nailong He[2], Sen Zhang[2], Wentong Zhang[1], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Technology Development Department, CSMC Technologies Corporation, China; [3]Wuxi China Resources Microelectronics Co., Ltd., China

C4P-C SiC-P1: SiC Devices (Poster Session)
Time: 15:30-17:00
Location: Poster
Chair(s): Ayanori Gatto, *Mitsubishi Electric*
Takaaki Tominaga, *Mitsubishi Electric*

C4P-C.1 Temperature-Dependent ESD Robustness in Micrometer 4H-SiC CMOS Technology
Pengyu Lai, Hui Wang, Kevin Chen, H. Alan Mantooth, Zhong Chen
University of Arkansas, United States

C4P-C.2 Bipolar Pre-Injection Phenomenon at Anomalously Low Anode Voltage in 4H-SiC RC-IGBT
Haizhao Zhi, Sirui Feng, Ling Li, Xinpeng Lin, Ying Dai, Yiling Li, Xinyue Dai, Xiaoping Wang, Yuxi Wan
Shenzhen Pinghu Laboratory, China

C4P-C.3 Parasitic BJT Activation and Punch-Through Mechanisms in a Hybrid-Drain Embedded SiC JFET
Haizhao Zhi, Sirui Feng, Ying Dai, Xinpeng Lin, Ling Li, Yiling Li, Xinyue Dai, Xiaoping Wang, Yuxi Wan
Shenzhen Pinghu Laboratory, China

C4P-C.4 Impact of Carbon Cap Defects on the Reliability of Automotive 1.2 kV SiC MOSFETs
Jinying Yu, Jingjing Cui, Jie Deng, Baocheng Yuan
Li Auto Inc., China

C4P-C.5 Demonstration of a Monolithically Integrated SiC Double-RESURF MOSFET Half-Bridge
Junze Li[1], Qing Guo[1], Jiazeng Ren[1], Zijian Hu[1], Jingkai Lin[1], Genyuan Yang[1], Zhen Zhang[1], Jiangbin Wan[1], Hai Lin[2], Hengyu Wang[1], Na Ren[1], Kuang Sheng[1]
[1]College of Electrical Engineering, Zhejiang Key Laboratory of Advanced Micro-nano Transducers Technology, Zhejiang Univ., China; [2]Shaoxing Institute of Zhejiang Univ., China

C4P-C.6 Reliability of SiC SBD Edge Terminations Under HV-H3TRB and Thermal Cycling Tests
Kouta Abe, Hiroshi Yano, Noriyuki Iwamuro
University of Tsukuba, Japan

C4P-C.7 On the Impact of Gate Switching Instability in Switching Performance for SiC Trench MOSFETs
Jaume Roig[1], Rishi Krishna[2], Agnimitra Saha[2], Sotirios Maslougkas[2], Nikolas Masnicak[3], Tanuj Saxena[4]
[1]onsemi, Belgium; [2]onsemi, Sweden; [3]onsemi, Czechia; [4]onsemi, United States

C4P-C.8 Experimental Study on Reverse Conduction FinFET with Integrated Junctionless Diode
Kaiwei Dai[1], Yuxi Wei[1], Chaoyu Gong[1], Jialei Tan[1], Jie Wei[1], Bo Zhang[1], Xiaorong Luo[1,2]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, Engineering Research Center of Advanced Power and RF Devices and Integration of Ministry of Education, University of Electronic Science and Technology of China, China; [2]School of Communication Engineering (School of Microelectronics), Chengdu University of Information Technology, China

C4P-C.9 A Novel 4H-SiC Trench MOSFET with Self-Adaptive Potential P-Shield for Excellent Trade-Off Between Conduction Loss and Robustness
Xiangrui Fan[1], Haozhu Pei[1], Jing He[1], Zitao Lin[1], Jiameng Sun[2], Yiren Yu[1], Yu Tian[1], Junhou Cao[1], Zhaoxiang Wei[1], Qian Wang[2], Long Zhang[1], Jiaxing Wei[1], Siyang Liu[1], Weifeng Sun[1]
[1]National ASIC System Engineering Research Center, School of Integrated Circuits, Southeast University, China; [2]Yangjie Electronic Technology Company Ltd., China

C4P-C.10 Design Constraints for a Si/SiC Fusion Switch with Realistic Boundary Conditions
M.S. Weidl, F. Wolter, T. Reiter, C. Ouvrard, A. Philippou, N.M. Muenzer, M. Niendorf, W. Jakobi
Infineon Technologies AG, Germany

C4P-C.11 SiC MOSFET with Two Embedded Series-Opposed Polysilicon Diodes for Improved Short-Circuit Capability
Yijiang Liu, Ruifeng Yue, Xiaosen Liu, Yan Wang
Tsinghua University, China

C4P-C.12 High Performance Monolithic Integration of 20 V CMOS Gate Driver and 1.7 kV JBSFET on 4H-SiC
Yu-Chin Ting[1], Quan-Han Chen[1], Ming-Han Wang[1], Chia-Lung Hung[2], Yi-Kai Hsiao[2], Bing Yue Tsui[1]
[1]Institute of Electronics, National Yang Ming Chiao Tung University, Taiwan; [2]Hon Hai Research Institute, Taiwan

C4P-C.13 Thermal Management of Parallel SiC MOSFETs Using Time-Domain Gate Resistance Modulation
Yuchu Ge[1], Xiangyu Teng[1], Xin Ming[2], Wei Jia Zhang[1]
[1]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, China; [2]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China

C4P-C.14 Distributed Model for Capacitance-Based Extraction of Channel and Drift Resistance in SiC MOSFETs
Tanuj Saxena[1], Rishi Krishna[2], Jaume Roig[3]
[1]onsemi, United States; [2]onsemi, Sweden; [3]onsemi, Belgium

C4P-C.15 A Behavioral Model for Pulse Generator Based on Series-Connected SiC DSRDs
Ziwen Chen, Yuxiao Yang, Yao Yang, Ruize Sun, Wanjun Chen, Bo Zhang
University of Electronic Science and Tech. of China, China

C4P-C.16 Performance Comparison of Standalone 4H-SiC JFETs and Cascode Devices at Cryogenic Temperature
Yiren Yu, Ziyan Miao, Jiaxin Zhai, Jiayi Shen, Xiangrui Fan, Yu Tian, Zhaoxu Song, Jiaxing Wei, Siyang Liu, Weifeng Sun
National ASIC System Engineering Research Center, Southeast University, China

C4P-C.17 Bipolar Behavior of SiC MOSFETs with Charge-Balance-Assisted Structures

Yuhan Duan[1,2], Liming Che[1,2], Botao Sun[3], Yuanlan Zhang[3], Pan Liu[1,2], Guangyin Lei[1], Min Li[1], Qingchun Jon Zhang[1]
[1]College of Intelligent Robotics and Advanced Manufacturing, Fudan University, China; [2]Research Institute of Fudan University in Ningbo, China; [3]SiChain Semiconductors (Ningbo) Co., Ltd., China

C4P-D SiC-P2: SiC Devices (Poster Session)

Time: 15:30-17:00
Location: Poster
Chair(s): Ayanori Gatto, *Mitsubishi Electric*
Fisher Craig, *Vishay*

C4P-D.1 A Coupled-Charge Driven Reverse-Recovery SPICE Model for SiC MOSFETs Considering Quasi-Floating Channel Effects

Fu-Jen Hsu[1,2], Ting-Fu Chang[1], Hsiang-Ting Hung[1], Chung-Ju Yu[1], Chih-Fang Huang[2], Cheng-Tyng Yen[1]
[1]Fast SiC Semiconductor Incorporated, Taiwan; [2]National Tsing Hua University, Taiwan

C4P-D.2 Geometry Scalable SPICE Modeling of 4H-SiC CMOS for Integrated Circuit Design

Shuqiang Chen[1], Yong Gu[1], Mengyao Zhao[1], Yu Huang[2], Runhua Huang[2], Song Bai[2], Jie Ma[1], Weifeng Sun[1], Long Zhang[1]
[1]National ASIC System Engineering Research Center, School of Integrated Circuits, Southeast University, China; [2]Nanjing Electronic Device Institute, China

C4P-D.3 A New 1200V SiC Trench MOSFET with Shallow Trench and High-Energy Deep P^+ Implantation for Enhanced Gate Oxide Electric Field Shielding

Moufu Kong[1], Zhaoyu Ai[1], Hongfei Deng[1], Qizhi Feng[1], Mingliang Yang[1], Xuebing Yin[2], Bingke Zhang[3]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices of China, University of Electronic Science and Technology of China, China; [2]Hubei Jiufengshan Laboratory, China; [3]Leshan Share Electronic Co., Ltd., China

C4P-D.4 Negative Temperature Dependence of Reverse-Recovery Overshoot Voltage in LDG-FS SiC MOSFET Body Diodes

Qiming He, Zhong Lan, JianJie Xiao, Wei Liu, Cheng Liu, Huijie Zhang, Ling Li, Rongyu Xue, Qijun Liu, Guan Song, Pengxiang Wang, Yafei Wang, Yao Yao, Chengzhan Li, Qiang Xiao, Haihui Luo
Zhuzhou CRRC Times Electric Co., Ltd., China

C4P-D.5 Design and Fabrication of 1 cm² Chip Size, 20kV Rated SiC MOSFETs on 200 mm SiC Wafer

Yun Xia[1], Gang Chen[1], Wei Liu[1], Yitian Jiang[1], Ying Dai[1], Lei Song[2], Jinliang He[2], Zheqian Chen[2], Bo Liao[2], Chiteng Deng[2], Haifeng Hou[2], Rongxin Du[1], Jinghan Xu[1], Jiamin Tian[1], Xiong Yang[1], Yuxi Wan[1]
[1]Shenzhen Pinghu Laboratory, China; [2]Shenzhen Pengjin High-Tech Co., Ltd., China

C4P-D.6 Dynamic-Thermal Stress: A Critical Factor in Automotive SiC MOSFET Reliability and Lifetime Prediction

Jihong Zhu, Jingjing Cui, Jinying Yu, Baocheng Yuan
Li Auto Inc., China

C4P-D.7 First Investigation of Output Capacitance Loss in 4H-SiC Super-Junction Devices

Shuying Zhu[1], Hengyu Wang[1], Haoyuan Cheng[1], Yuhao Zhang[2], Runze Xia[1], Chi Zhang[1], Zixuan Zheng[1], Kuang Sheng[1]
[1]College of Electrical Engineering, Zhejiang University, China; [2]Department of Electrical and Electronic Engineering, The University of Hong Kong, China

C4P-D.8 Characterization, Analysis, and Modeling of Quasi-Saturation in High-Voltage Superjunction 4H-SiC Power DMOSFETs

Zhaowen He[1], Collin Hitchcock[2], Stacey Kennerly[2], Reza Ghandi[2], T. Paul Chow[1]
[1]Rensselaer Polytechnic Institute, United States; [2]GE Aerospace, United States

C4P-D.9 Influence of Interface Traps and Cell Design on Dynamic VSD Behaviour in Double-Trench SiC MOSFETs

Madhu Lakshman Mysore, Rahul-Vijaybhai Chavda, Maximilian Goller, Patrick Heimler, Thomas Basler
Chemnitz University of Technology, Germany

C4P-D.10 Single-Event Effects and Leakage Mechanisms in ATG SiC MOSFETs Under Off-State Drain Bias and On-State Gate Bias

Yanjun Li[1], Manyi Ji[2], Lingxu Kong[2], Hongyi Xu[3], Li Liu[4], Jiupeng Wu[1], Na Ren[2]
[1]ZJU-Hangzhou Global Scientific and Technological Innovation Center, Zhejiang University, China; [2]College of Electrical Engineering, Zhejiang University, China; [3]Silicon Magic Semiconductor Technology Co., Ltd., China; [4]School of Engineering, Huzhou University, China

C4P-D.11 Repetitive Avalanche Pulses of SiC Trench MOSFETs During First and Third Quadrant Operation
Sebnem Tuncay[1], Dethard Peters[1], Thomas Basler[2]
[1]Infineon Technologies AG, Germany; [2]Chemnitz University of Technology, Germany

C4P-D.12 Influence of JFET Region Design on the Repetitive Short-Circuit Ruggedness in Trench SiC MOSFETs
Katsuhisa Tanaka, Yuji Kusumoto, Masataka Yukumoto, Tsutomu Kiyosawa, Hiroshi Kono, Takuma Suzuki, Kenya Sano
Toshiba Electronic Devices & Storage Corporation, Japan

C4P-D.13 Surge Capability of 3.3 kV SBD-Embedded SiC MOSFETs and Impact of the SBD Layout
Zijian Hu[1,2], Yuanying Li[1], Hongyi Xu[3], Jiupeng Wu[2], Junze Li[1], Chi Zhang[1], Liming Wei[4], Shichao Jiang[5], Youquan Zhang[5], Wei Liu[5], Lei Chen[5], Na Ren[1,2]
[1]College of Electrical Engineering, Zhejiang University, China; [2]Institute of Advanced Semiconductors, ZJU-Hangzhou Global Scientific and Technological Innovation Center, China; [3]Silicon Magic Semiconductor Technology Co., Ltd., China; [4]Semichase Semiconductor Technology Co., Ltd., China; [5]Hangzhou Firstack Technology Co., Ltd., China

C4P-D.14 Impact of Cell Orientation on 1.2 kV 4H-SiC MOSFETs with Channeling Implanted Deep P-Well
Dinuth C.Y.B. Yapa Mudiyanselage[1], Skylar Deboer[1], Stephen A. Mancini[1], Justin Lynch[2], Seung Yup Jang[2], Adam J. Morgan[2], Woongje Sung[1]
[1]State University of New York at Albany, United States; [2]NoMIS Power Corporation, United States

C4P-D.15 Analytic Modeling and Transient Characterization of Fast-Recovering Gate Oxide Defects in SiC MOSFETs
Xu Li[1], Yaoxin Lin[2], Jian Chen[1], Haitao Liu[3], Wensheng Song[1]
[1]School of Integrated Circuit Science and Engineering, Southwest Jiaotong University, China; [2]School of Electrical Engineering, Southwest Jiaotong University, China; [3]CRRC Zhuzhou Electric Locomotive Research Institute Co., Ltd., China

C4P-D.16 1.2 kV 3D Quasi-Planar Trench SiC MOSFET with P-Body Layer as Trench Protection
Mansha Kansal[1], Iulian Nistor[2], Kyrylo Melnyk[3], Giuseppe Capasso[1], Alessandro Borghese[1], Michele Riccio[1], Arne Benjamin Renz[3], Giovanni Breglio[1], Neophytos Lophitis[4], Andrea Irace[1], Marina Antoniou[3], Munaf Rahimo[2], Luca Maresca[1]
[1]Department of Electrical Engineering and Information Technology, University of Naples Federico II, Italy; [2]mqSemi AG, Switzerland; [3]School of Engineering, University of Warwick, United Kingdom; [4]Faculty of Engineering and Technology, Cyprus University of Technology, Cyprus

C4P-D.17 Third-Quadrant Characteristic and Surge Current Behavior of SiC MOSFET at Different Conduction Modes
Xu Li[1], Xiaochuan Deng[2], Xuan Li[2], Jiahao Hu[2], Wensheng Song[1]
[1]Southwest Jiaotong University, China; [2]University of Electronic Science and Technology of China, China

C4P-D.18 Novel Short-Circuit Failure Mechanisms of Trench SiC MOSFETs Suffering Total Ionizing Dose
Hanqing Zhao[1], Jiahao Hu[1], Jinggui Zhou[1], Ruizhe Sun[2], Yifan Wu[3], Hanyi Zheng[1], Cheng Yang[1], Xuan Li[1], Xiaochuan Deng[1], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Institute of Engineering Electronics, China Academy of Engineering Physics, China; [3]Shanghai Belling Corp., Ltd., China

C4P-E PK-P: Packaging Technologies (Poster Session)
Time: 15:30-17:00
Location: Poster
Chair(s): Ayanori Gatto, *Mitsubishi Electric*
Takaaki Tominaga, *Mitsubishi Electric*

C4P-E.1 Detecting Asymmetries Within Multi-Chip SiC Power Modules by Means of the Kelvin Source
Jonas Müller[1], Hauke Lutzen[1], Torben Buchholz[1], Jan-Hendrik Peters[1], Wataru Saito[2], Nando Kaminski[1]
[1]University of Bremen, Germany; [2]Kyushu University, Japan

C4P-E.2 Development of the 500kVA/L Ultra-High Power Density Next-Generation SiC Inverter Unit
Yoshihiro Tateishi, Keita Suzuki, Satoharu Tanai, Akira Kitamura, Tetsuo Endoh, Yoshikazu Takahashi
Tohoku University, Japan

C4P-F GaN-P2: GaN Devices (Poster Session)
Time: 15:30-17:00
Location: Poster
Chair(s): Ayanori Gatto, *Mitsubishi Electric*
Fisher Craig, *Vishay*

C4P-F.1 Design and Development of High-Current E-Mode GaN p-FET and Complementary Logic Circuits on UID-GaN/AlGaN Platform
Xuanming Zhang[1,2], Yunsong Xu[1,2], Jiachen Duan[1,2], Haotian Ji[1,2], Jun Wen[2,3], Zhiwei Sun[4], Zifeng Qu[1,2], Jiangmin Gu[1,2], Ye Liang[1,2], Ivona Mitrovic[2], Harm van Zalinge[2], Jie Zhang[2,3], Xi Chen[1,2], Sen Huang[5], Wen Liu[1,2]
[1]School of Advanced Technology, Xi'an Jiaotong-Liverpool University, China; [2]Department of Electrical Engineering and Electronics, University of Liverpool, United Kingdom; [3]School of Chips, Xi'an Jiaotong-Liverpool University, China; [4]Suzhou Laboratory, China; [5]Department of High-Frequency and High-Voltage Devices, University of Chinese Academy of Sciences, China

C4P-F.2 Substrate Management for GaN Bi-Directional Switch Based on Charge Recycling of Slow Recovery Diode
Junjie Zhu[1], Zongjie Zhou[1], Junting Chen[1], Ji Shu[1], Zheng Wu[1], Tao Chen[1], Yuwei Wu[1], Yan Cheng[1], Yutao Geng[1], Longge Deng[1], Yat Hon Ng[1], Gaofei Tang[2], Qimeng Jiang[2], Kevin J. Chen[1]
[1]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, China; [2]CloudSemi Technology Co., Ltd., China

C4P-F.3 Achieving Robust Single-Event Irradiation Tolerance in 6-Inch E-Mode GaN-on-Sapphire HEMTs with a Thin AlN Buffer
Can Zou[1,2], Yan Ma[1], Yiteng Yu[1], Zhengxiang Tang[1], Tianqi Wang[3], Jianli Liu[3], Zhengliang Zhang[3], Zheng Zhang[4], Liuxing Dai[5], Yuanyang Xia[6], Leke Wu[6], Yiheng Li[6], Tinggang Zhu[6], Weizong Xu[1], Dunjun Chen[1], Rong Zhang[1], Feng Zhou[1,2], Hai Lu[1]
[1]School of Electronic Science and Engineering, Nanjing University, China; [2]Shenzhen Research Institute of Nanjing University, China; [3]Space Environment Simulation Research Infrastructure (SESRI), Harbin Institute of Technology, China; [4]Department of Nuclear Physics, China Institute of Atomic Energy, China; [5]Gushi (Suzhou) Technology Co., Ltd., China; [6]CorEnergy Semiconductor Co., Ltd., China

C4P-F.4 Drain Voltage Stress Timing Strategy Towards GaN HEMTs Dynamic RON Stability Mechanism
Zesen Chen[1], Zhengyu Chen[1], Ying Wang[1], Zhuoran Luo[1], Tian Luo[1], Wenkang Ji[1], Qianshu Wu[1], Tao Su[1], Yang Liu[1,2]
[1]School of Electronics and Information Technology, Sun Yat-Sen University, China; [2]Sun Yat-Sen University Shenzhen Research Institute, China

C4P-F.5 Visualizing the Internal Discharging Current in GaN Power HEMTs During Switching Transients
Yuan Meng[1], Chi Wang[1], Yang Dong[1], Junsong Jiang[2], Li Zhang[3], Xi Tang[2], Shibing Long[1], Zheyang Zheng[1]
[1]School of Microelectronics, University of Science and Technology of China, China; [2]Institute of Physical Science and Information Technology, Anhui University, China; [3]Silergy Corp., China

C4P-F.6 kV-Class Photoconductive Semiconductor Switches Using Mn-Doped Semi-Insulating GaN Bulk Crystals
Takuya Maeda[1], Chinwei Li[1], Ryosho Nakane[1], Kenji Iso[2]
[1]University of Tokyo, Japan; [2]Mitsubishi Chemical Co., Japan

C4P-F.7 Frequency Dependence of p-GaN Gate Lifetime Evaluated Under Realistic Driver-Loop Stress
Sijiang Wu, Siyuan Ye, Zhiyong Liang, Shanshan Wang, Haohao Chen, Zhaojun Liu, Junmin Jiang, Mengyuan Hua
Southern University of Science and Technology, China

C4P-F.8 3 kV, 982 MW/cm² Monolithic GaN Bidirectional Switch with Tunneling Layer Fin-Gate and Dual-Passivated p-GaN/Schottky Hybrid Drain
Yizhou Jiang[1,2], Huiqing Wen[1,2], Zifeng Qu[1,2], Hao Tian[1,2], Xuanming Zhang[1,2], Jiachen Duan[1,2], Wen Liu[1,2]
[1]Xi'an Jiaotong-Liverpool University, China; [2]University of Liverpool, United Kingdom

C4P-F.9 Investigation of the Gate Leakage Current of Schottky-Type p-GaN Gate HEMTs During SC-Events
Tim Egener, Christoph Schmickler, Jorge Perez, Martin Pfost
Technical University of Dortmund, Germany

C4P-F.10 Ultra-Wide Bandgap Al0.85Ga0.15N/Al0.65Ga0.35N HEMTs with Baliga Figure of Merit > 0.5 GW/cm² Leveraging LPCVD SixNy Passivation and Field Plates
Aditya Varma[1], Seungheon Shin[2], Joseph McGlone[2], Patrick Darmawi-Iskandar[1], Hridibrata Pal[1], Zhongyunshen Zhu[1], Yinxuan Zhu[2], Tariq Jamil[3], S.M Tazbiul Hasan[3], Abdullah Al Mamun Mazumder[3], Chandan Joishi[4], James Fiorenza[4], Siddharth Rajan[2], Asif Khan[3], Tomás Palacios[1]
[1]Microsystems Technology Laboratories, Massachusetts Institute of Technology, United States; [2]Department of Electrical and Computer Engineering, The Ohio State University, United States; [3]Department of Electrical Engineering, University of South Carolina, United States; [4]Analog Devices Incorporated, United States

C4P-F.11 Gate/Drain Stress Interplay in Low-Voltage Schottky-Type p-GaN Gate HEMTs During Switching Operation
Longge Deng, Yuwei Wu, Junting Chen, Tao Chen, Yan Cheng, Ji Shu, Zheng Wu, Yat Hon Ng, Kevin J. Chen
The Hong Kong University of Science and Technology, China

C4P-F.12 Investigation of Field Plate Design and Gate Control Strategies for Monolithic Bidirectional GaN HEMTs in Vienna Rectifier Applications
Chun-Hao Lai, Wei-Ting Hsu, Vito Argono, Po-Yen Huang, Haoran Wang, Xi Jie Lim, Shawn S. H. Hsu, Roy K.-Y. Wong
National Tsing Hua University, Taiwan

C4P-F.13 System-Level Evaluation of Dead-Time Loss Induced by Dynamic Threshold Voltage of GaN HEMTs
Yuwei Wu, Zhaotian Yan, Jiaheng He, Kevin J. Chen
The Hong Kong University of Science and Technology, China

C4P-F.14 Demonstration of High Voltage (>1.7kV) GaN Negative-Capacitance Ferroelectric HEMTs Using HZO Gate Stack Achieving 47.89 mV/dec SS and Reduced ON-Resistance
Thi My Hanh Dao, Yu-An Chen, Hsien-Yang Liu, Tian-Li Wu
National Yang Ming Chiao Tung University, Taiwan

C4P-F.15 γ-Ray Irradiation-Induced Dynamic RON Degradation in P-GaN Gate HEMT: Role of Surface Trapping
Chenyue Chu[1], Xuan Xie[1], Juntai Wang[1], Ziang Wang[1], Minze Wang[1], Hao Zhang[1], Xi Tang[2], Shibing Long[1], Shu Yang[1]
[1]University of Science and Technology of China, China; [2]Anhui University, China

C4P-F.16 450 V/18 mΩ Radiation Hardened P-GaN Gate HEMT with Single-Event Hardness at 82 MeV·cm²/mg
Xuan Xie[1], Minze Wang[1], Ziang Wang[1], Zhi Wang[1], Yawen Zhang[1], Qiuyi Tang[1], Chenyue Chu[1], Guangwei Xu[1], Shibing Long[1], Bo Shen[2], Shu Yang[1]
[1]University of Science and Technology of China, China; [2]Peking University, China

C4P-F.17 Monolithic Integration of E/D-Mode Power HEMTs and Self-Powered Circuits on a Standard GaN Platform
Fengping Lin[1], Gaofei Tang[2], Yao Chen[1], Zhiwen Dong[2], Hongfeng Chen[1], Junsong Jiang[1], Xiaoyu Liu[1], Chenyue Chu[3], Zhaofu Zhang[4], Shu Yang[3], Xi Tang[1]
[1]Institute of Physical Science and Information Technology, Anhui University, China; [2]CloudSemi Technology Company Ltd., China; [3]School of Microelectronics, University of Science and Technology of China, China; [4]School of Integrated Circuits, Wuhan University, China

C4P-F.18 Revisiting the Avalanche Breakdown Criterion in High-Dislocation-Density GaN Power Devices
Zineng Yang[1], Yifan Wang[2], Hehe Gong[1], Jiaqi He[3], Hang-Ming Zhang[1], Kai Cheng[3], Han Wang[1], Yuhao Zhang[1]
[1]Centre for Advanced Semiconductors and Integrated Circuits and Dept. of Electrical and Computer Engineering, University of Hong Kong, China; [2]Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, United States; [3]Enkris Semiconductor, Inc., China

Thursday, May 28, 2026

D1L-A SiC-3: Beyond Conventional Device Structures
Time: 8:40-10:00
Location: Lecture
Chair(s): Rahul Potera, *Alpha & Omega Semiconductor*
Cheng-Tyng Yen, *Fast SiC Semiconductor*

8:40
D1L-A.1 Investigation of Different Layout Designs for 4H-SiC MOSFETs with an Integrated Channel Diode
Stephen A. Mancini[1], Dinuth C.Y.B. Yapa Mudiyanselage[1], Seung Yup Jang[1,3], Andrew Binder[2], Richard Floyd[2], Robert Kaplar[2], Jack Flicker[2], Stan Atcitty[2], Justin Lynch[1], Adam J. Morgan[3], Woongje Sung[1]
[1]College of Nanotechnology Science and Engineering, University at Albany, United States; [2]Sandia National Labs, United States; [3]NoMIS Power Corp., United States

9:00

D1L-A.2 Smart 1.7 kV SiC Power ICs: Monolithic Integration of TCOX UMOSFETs and Tri-Gate CMOS

Chia-Lung Hung[1], Jing-Neng Yao[2], Yun-Ting Huang[3], Ho-Lin Kao[3], Bing-Yue Tsui[3], Tian-Li Wu[3], Yi-Kai Hsiao[1], Hao-Chung Kuo[1]
[1]Hon Hai Research Institute, Taiwan; [2]Hon Young Semiconductor Corporation, Taiwan; [3]National Yang Ming Chiao Tung University, Taiwan

9:20

D1L-A.3 An 850V Gate Driver Integrated 4H-SiC Planar MOSFET SiP with 560MW/cm² BFOM And 10MHz High-Speed Switching Capability

Fu-Jen Hsu[1,2], Hsiang-Ting Hung[1], Ting-Fu Chang[1], Chung-Ju Yu[1], Chih-Fang Huang[2], Cheng-Tyng Yen[1]
[1]Fast SiC Semiconductor Incorporated, Taiwan; [2]National Tsing Hua University, Taiwan

9:40

D1L-A.4 Superior Third Quadrant Performance in Ultra Narrow 4H-SiC Vertical FinFETs

Q. Wang[1], N. Donato[1], F. Udrea[1], H. Alan Fujioka[2], T. Kumazawa[2], H. Tomita[2], M. Okuda[2], T. Nishiwaki[2], H. Fujiwara[2], T. Kimoto[3]
[1]University of Cambridge, United Kingdom; [2]MIRISE Technologies Corporation, Japan; [3]Kyoto University, Japan

D2L-A GaN-3: GaN Power Device Reliability and Systems

Time: 10:20-12:00
Location: Lecture
Chair(s): Kwang Young Ko, *DB HiTek*
Yasuhiro Uemoto, *Infineon Tecnologies*

10:20

D2L-A.1 Enhanced Gate Reliability and High Threshold Voltage p-GaN HEMT with p-NiO/p-GaN Heterojunction

Jinbing Wang[1], Maojun Wang[1], Pengfei Wang[1], Jin Wei[1], Jinyan Wang[1], Xinyi Pei[2], Na Sun[2], Jiandong Ye[2], Xun Zhang[3], Yuxia Feng[3], Han Yang[4], Bo Shen[4]
[1]School of Integrated Circuits, Peking University, China; [2]School of Electronic Science and Engineering, Nanjing University, China; [3]College of Microelectronics, Beijing University of Technology, China; [4]School of Physics, Peking University, China

10:40

D2L-A.2 A Systematic Study of Total Ionizing Dose Effects on P-GaN Gate HEMTs Under Off-State Bias

Zhao Wang[1], Shuai Yuan[1], Shenghuai Liu[1], Ming Qiao[1,2], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, China; [2]Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, China

11:00

D2L-A.3 Under 10 Nanosecond Switching of 700V GaNFET Using a Chip-on-Board Optical Gate Drive

Khush Gohel, Hardik Chhabra, Yanwen Gu, Bowen Yang, Giri Venkataramanan, Chirag Gupta
University of Wisconsin-Madison, United States

11:20

D2L-A.4 Verification of Buck Converter via Optimized Monolithic Heterogeneous GaN/Si CMOS Process

Wenzhang Du[1], Xiaojun Fu[3], Junfeng Yu[1], Chunlei Wu[1], David Wei Zhang[1], Hongping Ma[4], Qingchun Zhang[4], Chen Qian[3], Guangsheng Zhang[3], Hong Zhou[5], Jincheng Zhang[5], HaiOu Li[6], Liang Li[7], Yuan Wang[8], Yue-Chan Kong[8], Xiaotian Fei[2], Pengcheng Yu[2], Xiaofeng Gu[2], Linna Zhao[2], Wei Huang[2]
[1]State Key Laboratory of Integrated Chips and Systems, Fudan University, China; [2]School of Integrated Circuits, Jiangsu Provincial Key Laboratory of MEMS Sensors and ASIC Manufacturing Technology, Jiangnan University, China; [3]National Key Laboratory of Integrated Circuits and Microsystems, China; [4]School of Academy for Engineering & Technology, Fudan University, China; [5]School of Microelectronics, Xidian University, China; [6]Guilin University of Electronic Technology, China; [7]School of Electronic Information Engineering, Suzhou Vocational University, China; [8]Nanjing Electronic Devices Institute, China

11:40

D2L-A.5 Slew-Rate Control of Dmode GaN Switches: Theory and Application

G. Gupta[1], N. Singh[1], J. Choi[1], P. Lai[2], Y. Huang[1], A. Ekbote[1], R. Lal[1]
[1]Renesas Electronics America, United States; [2]Renesas Electronics Hong Kong, China

D3L-A LVT-2: Low Voltage Vertical Devices
Time: 13:30-14:50
Location: Lecture
Chair(s): Xin Lin, *NXP Semiconductors*
Kwang Young Ko, *DB HiTek*

13:30
D3L-A.1 Power MOSFETs with Super Safe-Operating-Area
Mark Gajda, Ali Ghasemi, Hamza Patel
Nexperia B.V., United Kingdom

13:50
D3L-A.2 Super Q – A Revolution in Superjunction Technology
Phil Rutter, Haian Lin, Zia Hossain, David Jauregui
iDEAL Semiconductor Devices, Inc., United States

14:10
D3L-A.3 A Novel 40V High-Performance Lateral Power MOSFET Using a Charge-Coupled Trench Architecture
Stefano Zoino[1], Lia Masoero[1], Nicolas Pons[1], Ibtihale Boufous[1], Filippo Privitera[2], Rosalia Germana[1], Patrick Calenzo[1], Marina Ruggeri[1], Antonia Conte[3], Carlo Sportato[3], Monica Petralia[3], Guillaume Neyroz[1], Philippe Bienvenu[1], Sylvain Coquel[1], Stephane Amat[1], Julia Castellan[1], Antonio Calandra[1], Giuseppe Bonaventura[1], Philippe Sirito-Olivier[1]
[1]STMicroelectronics, Global Technology Research & Development, GTR&D VIPOWER R&D, France;
[2]STMicroelectronics, Global Technology Research & Development, GTR&D VIPOWER R&D, Italy;
[3]STMicroelectronics, Front-End Manufacturing, CATANIA 8 OPERATIONS, Italy

14:30
D3L-A.4 Enhancing Split-Gate MOSFET Efficiency via Source Resistance and Layout Optimisation
Ali Ghasemi, Mark Gajda, Ian Stubbs
Nexperia B.V., United Kingdom

Closing Session

Thursday, May 28, 2026

Time: 14:50-15:20
Location: Lecture
Chair(s): David Sheridan, *Alpha & Omega Semiconductor*
Sameh Khalil, *Infineon*

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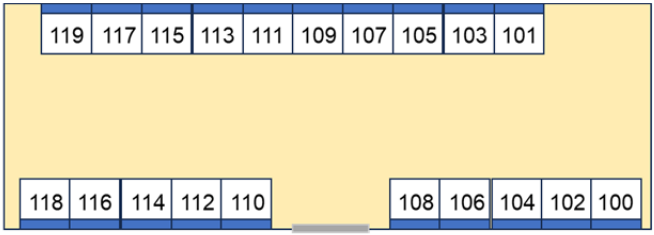

Chairman's Pre-Function Hallway

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Centrotherm	103
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The 39th International Symposium on Power Semiconductor Devices and ICs

ISPSD is the premier forum for technical discussions in all areas of power semiconductor devices and power integrated circuits, including but not limited to device physics, modeling, design, fabrication, materials, packaging and integration, device reliability, and device/circuit interactions.

ISPSD 2027 will be held in Taipei, Taiwan at the Taipei International Convention Center (TICC).

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Conference Submission Tracks:

- **High Voltage Devices (HV):** High voltage silicon based discrete devices (>200V) such as SJ-MOSFETs, IGBTs, thyristors and pn-diodes
- **Low Voltage Devices and Power IC Device Technology (LVT):** Low voltage silicon based discrete power devices (≤200V) and devices for power ICs of all voltage ranges
- **Power IC Design (ICD):** Circuit design and demonstration using power IC technology platform
- **GaN and Compound Materials:** GaN and nitride-based compound materials (e.g., AlN) based power devices, technology and integration, materials, and processing
- **SiC and Other Materials (SiC):** SiC and other material (e.g., Ga_2O_3, diamond) based power devices, technology and integration, materials, and processing
- **Module and Packaging Technologies (PK):** System integration in package module and package technology for discrete power devices and power ICs

Abstract Submission

Prospective authors should visit the ISPSD 2027 website: https://www.ispsd2027.com

- **Important Dates:**
  Dec 16, 2026: 4-page full paper submission
  Jan 29, 2027: Author notification
  Feb 19, 2027: Final submission deadline for final paper and copyright filing
  Please note: A 4-page full paper submission is required. There will be no late news session.
- **Template:**
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  Paper length: Maximum 4 pages
  Paper size: US Letter
  File format: Adobe PDF (.pdf)

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